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CONTROLLED INVERSION DEVICES

Harry Kroger, et al

Sperry Research Center

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CONTROLLED INVERSION DEVICES

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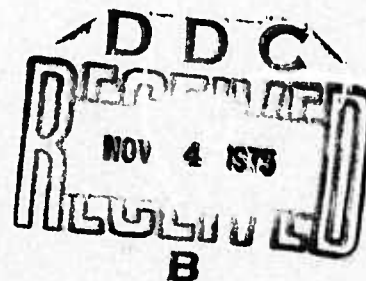Approved for public release; distribution unlimited.

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Three terminal controlled inversion devices were fabricated and the properties studied. Base current drive as low as 2 μA were sufficient to lower collector threshold voltages 0.6 V. Reliable switching of 100 mA currents was possible. Properties of devices fabricated of silicon nitride, silicon oxynitride and amorphous silicon as the thin insulator material were investigated. The reproducibility, lack of interaction between adjacent collector electrodes, and base current sensitivity of devices fabricated with polysilicon and amorphous suggest that further work on this material be emphasized. Devices fabricated with silicon nitride

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20. ABSTRACT (cont.)

and silicon oxynitride show a marked interaction between different collector electrodes on the same chip. Collector electrodes of the order of 0.1 cm apart can interact via a pulse applied to one electrode affecting the capability of a second electrode to make a transaction to the low impedance state for pulse applied up to 1 ms later. At low biases, about one third of the carriers crossing the silicon-rich nitride layers are electrons, while for the polysilicon layers the carriers are almost exclusively holes. High current density devices (5×10^3 A/cm^2 in low impedance state) have been fabricated which can handle as much as 0.5-1.0 A without damage. The impedance of the devices has been measured at microwave frequencies. These measurements indicate that the devices, when biased to the low impedance state, have a low resistance and a large reactive component between 1 and 10 GHz. The reactive component is sufficiently different between the low and high resistance states to make unambiguous identification of which state the device is residing. Measurements of device capacitance at 1 MHz, under full three-terminal bias conditions, demonstrate the development of an inversion layer when the collector is biased near the threshold voltage in its high impedance state. CID structures fabricated completely from polysilicon (with no single crystal silicon) have shown a nonvolatile memory effect.

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SECTION 1

INTRODUCTION

A. REVIEW OF PROPERTIES OF CONTROLLED INVERSION DEVICES

The controlled inversion device (CID) is a two- (or multiple-) terminal semiconductor device which exhibits, in general, two or three stable impedance states. A typical current voltage characteristic is shown in Fig. 1, which indicates, except for the intermediate conductivity state, a qualitative relationship with the characteristics of a typical silicon-controlled rectifier (SCR). The structure is, however, quite different from such devices. As illustrated in Fig. 2, the CID has, at most, one (and in some cases no) p-n junction, unlike that of the SCR which has three junctions.

The mechanism of operation of the CID depends upon the finite conductivity of the thin insulator or, more descriptively, the "nonlinear" conductor which, depending upon bias conditions, might or might not possess an inversion layer. A qualitative description of the device behavior has been presented for both the diode[1] and "emitter-base-collector" version of the three-terminal structure.[2] The present report will update the I-V characteristics of the three-terminal devices for this program, and it will be shown that it is possible to more simply describe these characteristics as well as to envision greater utility for the structure.

B. GOALS OF PROGRAM

The goals of this program are to:

1. Complete quantitative theory of CID operation, including switching mechanism.

2. Discover possible preferred form of nonlinear conductor and other structure variations.

3. Study structures which are compatible with LSI processing. The specific structures which will be evaluated will only be those fabricated in the course of studies in 1 and 2 above.

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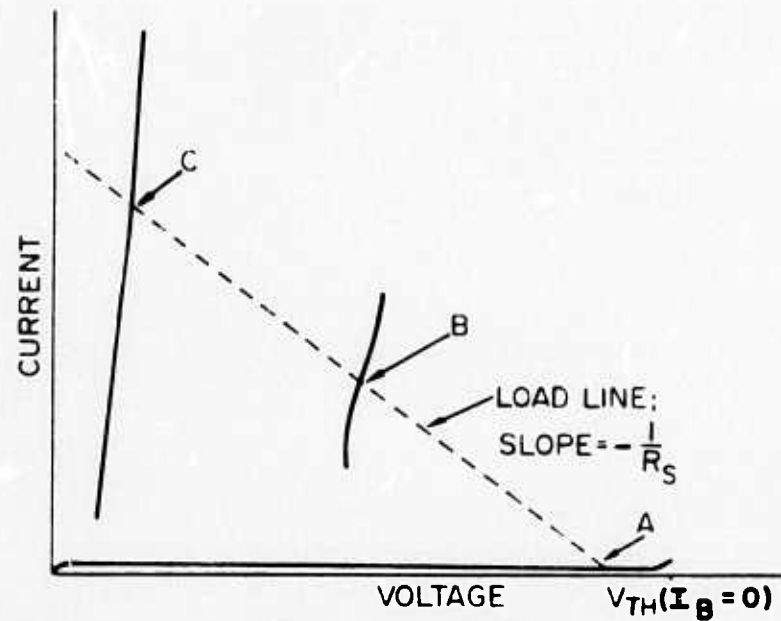
FIG. 1 Current voltage characteristics for a CID. If base current drive is
supplied threshold voltage V_{th} is reduced. Load line is determined
by series resistance of collector power supply. Switching from
$A \rightarrow B$, $B \rightarrow C$ or $A \rightarrow C$ is possible with base current drive.
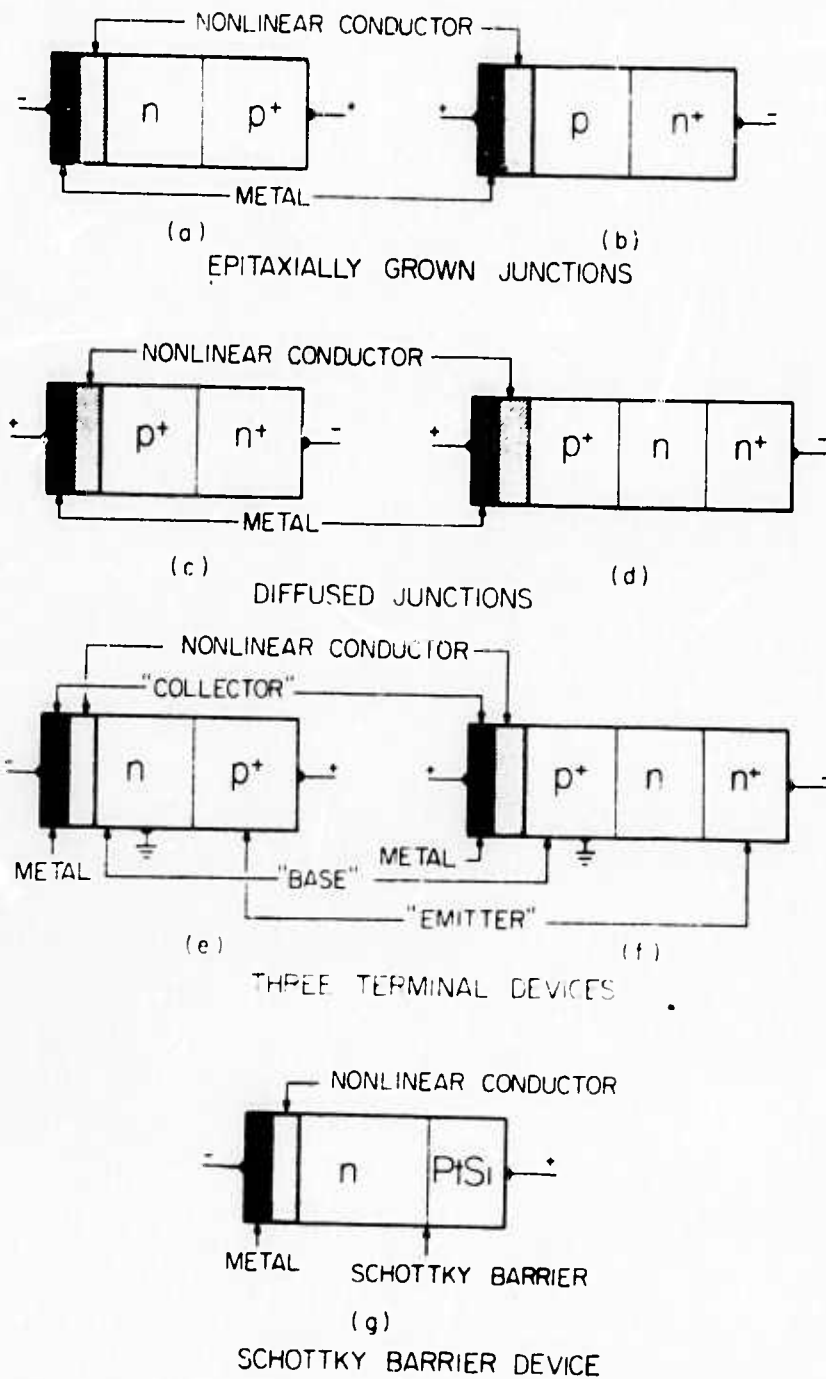
FIG. 2 Diagrams of controlled inversion device structures which have been fabricated at Sperry Research Center.

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4. Monitor reliability of devices throughout the program.

SECTION 2

THREE-TERMINAL DEVICES WITH "EMITTER-BASE-COLLECTOR"
(Silicon Nitride and Silicon Oxynitride Nonlinear Conductors)

A. STRUCTURES INVESTIGATED

Three-terminal structures, which had been fabricated at the time the proposal for this program was written, were conveniently fabricated but had nonideal base contacts. Two distinct structures were therefore initially investigated whose designs were supposed to greatly lower the base resistance by utilizing diffused base contacts.

(1) Structures Using Multiple Epitaxial Layer Structures.

Special silicon epitaxial layers were grown in order to provide a means of introducing a relatively low resistance base region adjacent to the junction. A cross sectional diagram of the wafer is shown in Fig. 3(a), and the sequential steps leading to complete device fabrication making use of limited area diffusions with oxide masking are illustrated in Figs. 3(b) and (c). Note that in this structure the diffused annular base contact region overlaps the more heavily diffused p layer adjacent to the p-n junction.

The "insulator" layer chosen for initial experimentation was 30 Å of silicon oxynitride. This specific composition was chosen because of its high and reproducible dielectric breakdown strength. Since the layer is thin, the possibility exists that tunneling can significantly contribute to conduction through the insulator.

(2) Diffused Base Contacts With Simple Epitaxial Layer.

A second structure investigated is illustrated in Fig. 4. It was fabricated from a simple p^-/n^+ epitaxial layer. This structure differed from the preceding one in two other respects: it was a mesa design which limited the emitter junction area and a 300 Å thick silicon-rich silicon-nitride insulator was used. The choice of this particular high conductivity material was motivated by a desire to observe if thicker insulator layers

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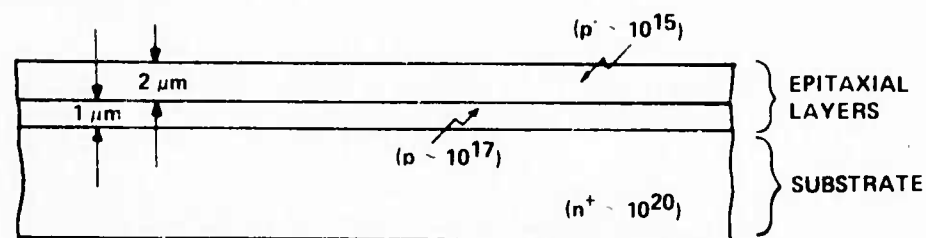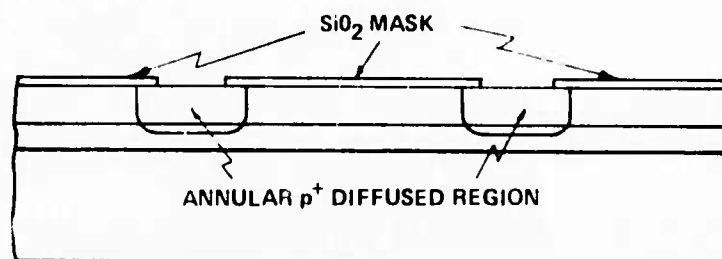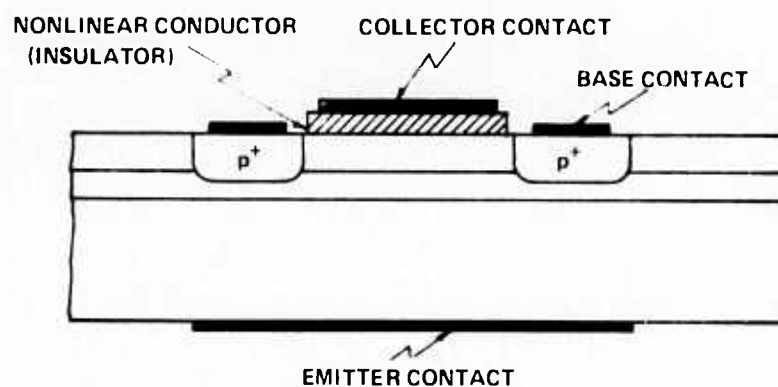
FIG. 3 Cross sectional view of emitter-base-collector CID fabricated from double epitaxial layer starting wafer.

(a) Original wafer.

(b) Similar base contact diffusion complete.

(c) Completed device.

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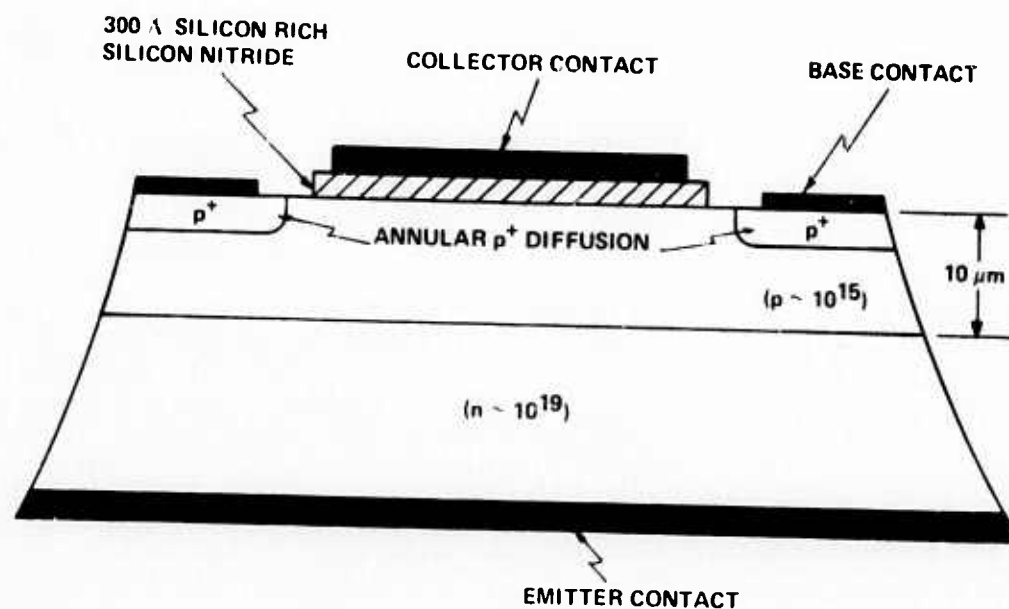
FIG. 4 Cross sectional view of emitter-base-collector CID fabricated using single epitaxial layer. Limited-area base contact diffusions are utilized along with a mesa etch to limit emitter junction area.

could result in more rugged devices and to examine the properties of devices whose conduction mechanism could not depend on tunneling directly from the semiconductor to the metal.

This structure did result in devices whose characteristics were less easily altered by high currents, and, as with the previous devices, multiple voltage levels in the low impedance states were not observed when different values of base current were supplied.

B. THRESHOLD VOLTAGE AS A FUNCTION OF BASE CURRENT

(1) Current Gain.

The structures in Figs. 3 and 4 showed substantial current gain when operated in the common emitter mode. Base currents 100-1000 times smaller than the collector current, which flowed after switching, could turn on the devices. The current gain is of course a function of the circuit, particularly of the collector load resistor, since the collector current is essentially limited by this resistance in the low impedance state. Earlier, three-terminal structures fabricated before the start of this program showed reliable current gains of only 6-10.

Figure 5 presents common emitter characteristics of the device diagrammed in Fig. 4. The peak collector current was over 200 mA and is not shown so that low currents of the high impedance state may be shown in detail.

(2) Measurements of $\Delta V_{th}/\Delta I_B$.

A useful figure of merit on the extent of control by base current I_B on collector threshold voltage V_{th} is the ratio $\Delta V_{th}/\Delta I_B$. If V_{th} is considered as a function of I_B, then the greater this ratio the more sensitive does the transition point depend upon base current.

Graphs of the base current vs threshold voltages are presented in Fig. 6 and 7 for the devices diagrammed in Figs. 3 and 4, respectively. Figure 6 contains data taken from three different devices which were representative of the devices examined. The maximum value of $\Delta V_{th}/VI_B$ was of the

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I → (0.5 mA/div.)

V → (2 V/div.)
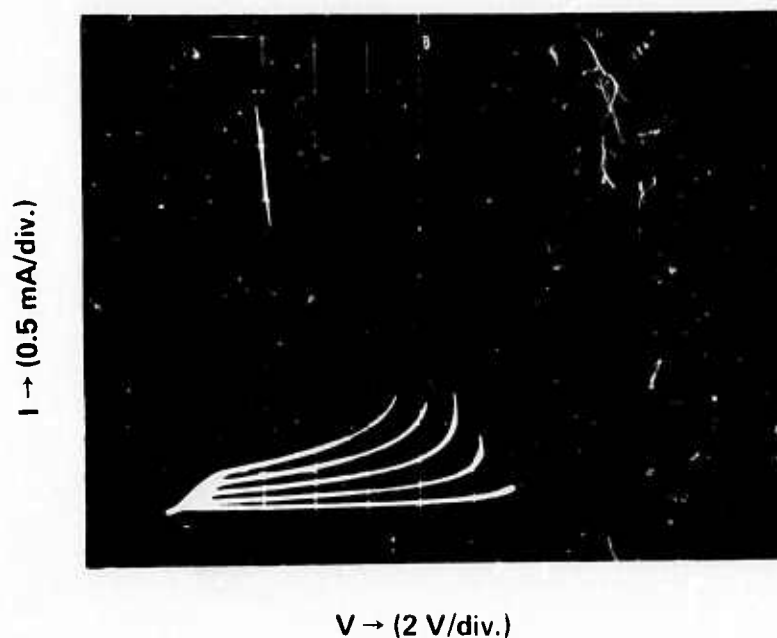
FIG. 5 Common emitter characteristics of device diagrammed in Fig. 4. The peak collector current is over 200 mA and is not shown so that low currents of high impedance state may be shown in detail. Four different curves correspond to base current I_B = 0, 0.1, 0.2 and 0.3 mA. Higher base currents lower collector threshold voltage.
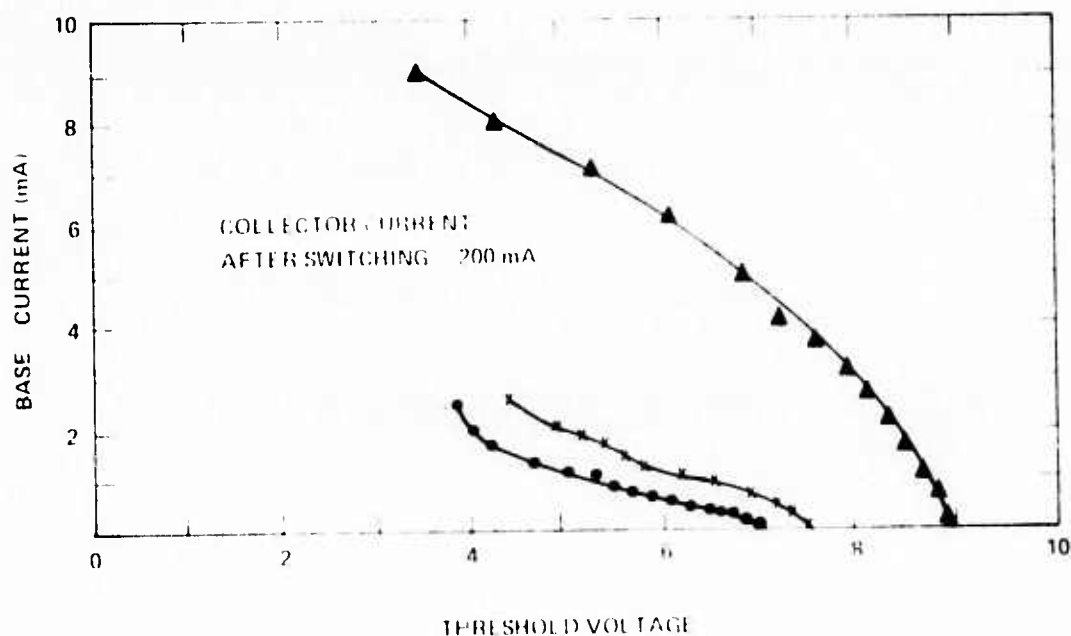
FIG. 6 Base current vs collector threshold voltage for device diagrammed in Fig. 3. Emitter is grounded.
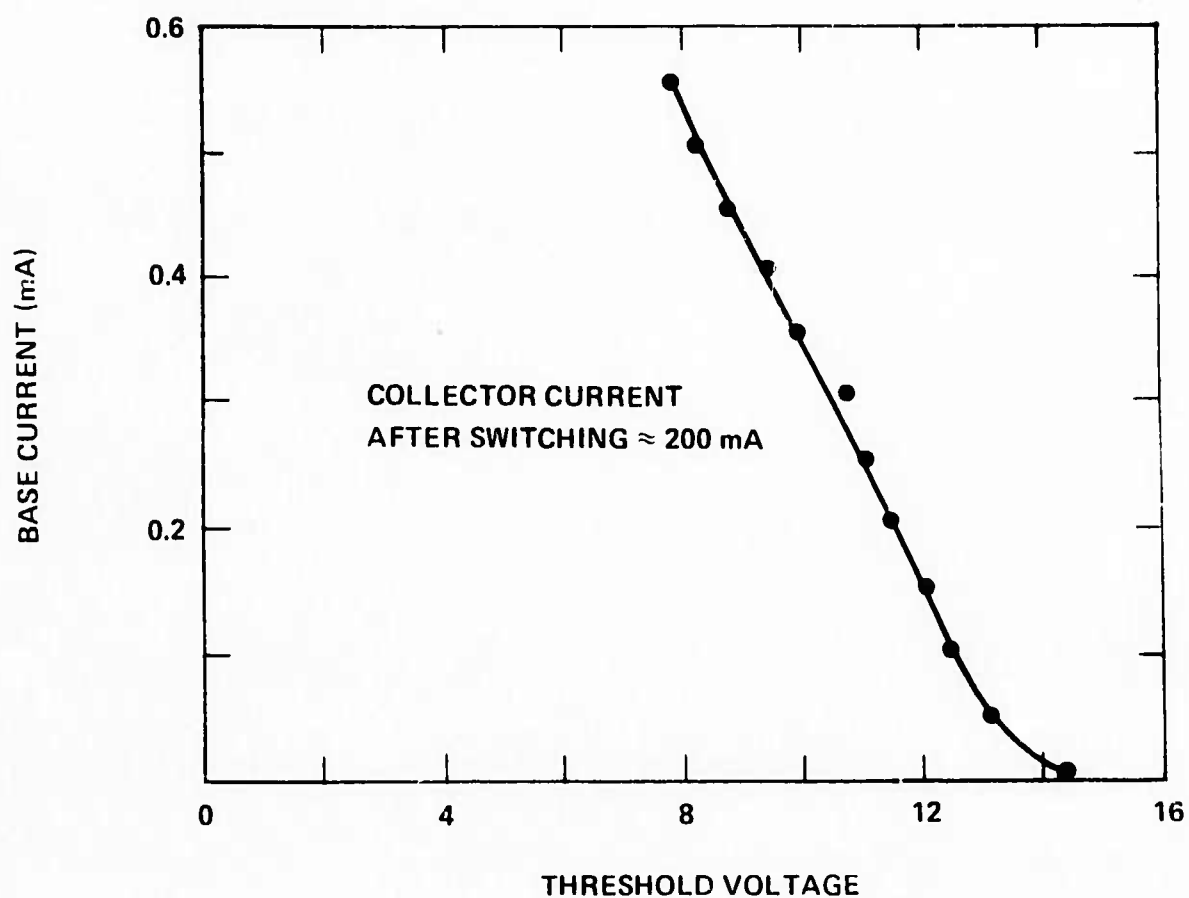
FIG. 7 Base current vs collector threshold voltage for device diagrammed in Fig. 4. Emitter is grounded.

order of 2000 Ω. The devices whose structure was diagrammed in Fig. 5, with the 300 Å nitride, were more alike in behavior. The data of Fig. 7 showed that for these devices $\Delta V_{th}/\Delta I_B \approx 12,000 \ \Omega$.

SECTION 3

CID STRUCTURES WITH POLYSILICON NONLINEAR CONDUCTORS

A. REVIEW OF PREVIOUS NLC MATERIALS

One of the striking facts about the CID phenomenon is its apparent universality. All insulator structures which have been used as the non-linear conductor in fabricating metal-NLC-semiconductor junction devices have exhibited the CID phenomenon. The insulators investigated prior to this contract included deposited layers of silicon oxynitride and silicon-rich silicon nitride, thermally grown silicon dioxide[3] and room-temperature grown SiO_x.

The silicon oxynitride which has been used was 20-35 Å thick of index of refraction 1.7 and was thin enough to permit some tunneling conduction. The current I through these layers measured in a simple metal-insulator heavily doped silicon structure showed a dependence[1] upon applied voltage V of the form

$$I = I_o \exp \frac{(\propto V)^{\frac{1}{2}}}{kT} \tag{1}$$

over five orders of applied voltage suggesting that tunneling was not the exclusive conduction mechanism. Such layers produced excellent devices only if molybdenum were used as the metal adjacent to the insulator (aluminum and chromium were also tried) and required deposition of the molybdenum immediately after the oxynitride deposition if the devices were to have a good yield.

The silicon-rich nitride was used in thickness from 175-300 Å. Chromium could be used successvully in the primary metallization but molyb-denum yielded more uniform devices. The metallization should be applied soon after deposition.

Layers of SiO_2 thermally grown at 550° C were also used successfully; however, only molybdenum metallization produced structures with high yield. Various "oxides" formed by heating silicon in NaOH and HNO_3 of $\approx$ 40 Å thickness have produced usable NLC layers for CID structures, but with a low yield ($<$ 80%).

B. METHODS OF FABRICATION AND BASIC PROPERTIES OF POLYSILICON CID STRUCTURES

Polycrystalline silicon layers were deposited and used in the fabrication of CID structures for the first time in a horizontal flow reaction at 700°C. The purpose of these experiments was to make use of the greater conductivity of polysilicon so that thicker "insulator" layers could be utilized, thus freeing the CID structure from the use of layers less than a few hundred angstroms thick.

Polysilicon layers, 2000 Å thick, were used and all devices showed the CID phenomenon. Several additional benefits and insights were reached using these devices beyond the most consistent and rugged performance observed to date. One interesting feature to the device behavior is the general absence of an intermediate conductivity state. Only the highest and lowest impedance states are present. The reasons for this behavior are not yet completely defined but may involve the fact that apparently only holes (not electrons) cross the polysilicon single-crystal silicon interface (see Fig. 8). All previous CID structures which did not use polysilicon as the insulator had a substantial fraction of current carried as both electrons and holes across the insulator semiconductor interface (ratio of electrons to holes $\approx$ 1/2).

A second interesting feature in the behavior of the polysilicon devices was observed only in the particular form of the devices diagrammed in Fig. 8(b). These devices had a double layer of polysilicon grown sequentially _in situ_. The first layer was an insulating polysilicon layer grown in argon as a carrier gas. The second layer was a conducting polysilicon layer using boron as the dopant and hydrogen as the carrier gas. The conductivity of this layer was approximately 3×10^{-3} Ω-cm. Both layers were 2000 Å thick.

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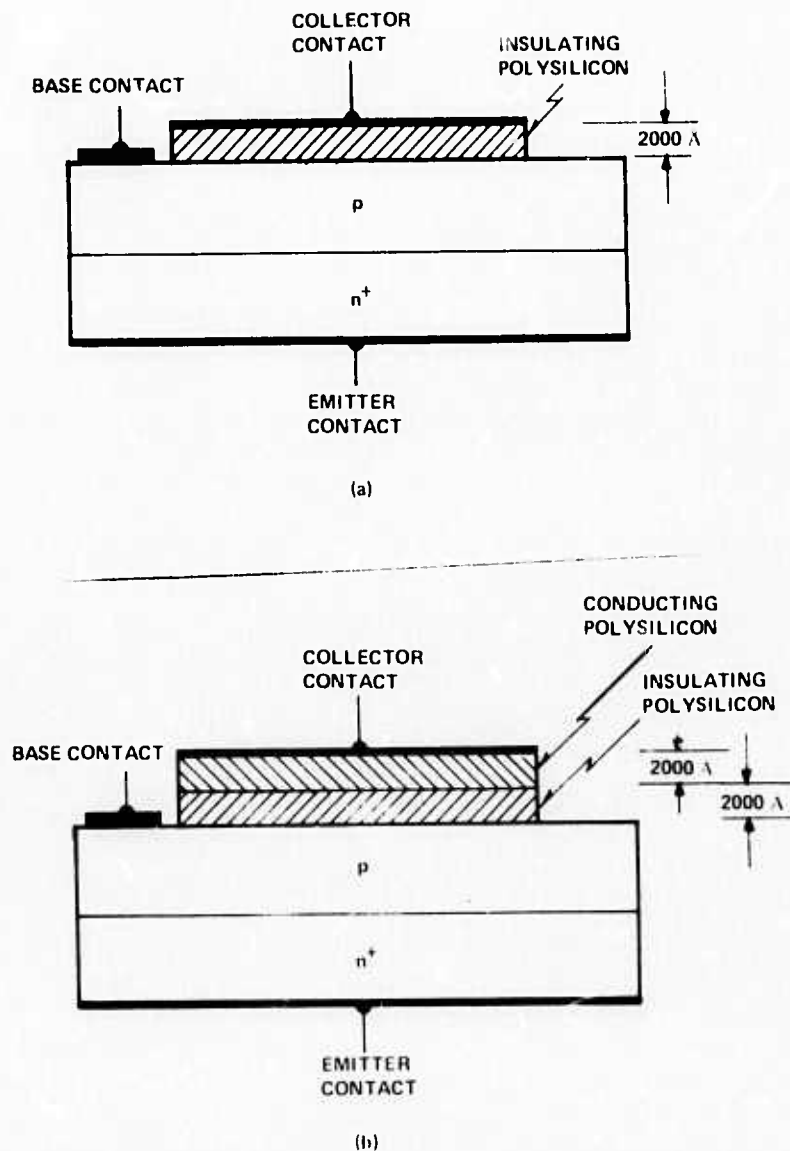
FIG. 8 Cross section diagram of CID structures fabricated with polysilicon:

(a) Single insulating polysilicon layer device.

(b) Double layer polysilicon device. Note that collector metalliza-
tion is not in contact with insulating layer.

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The double-layer polysilicon devices differed from all other CID's ever fabricated in that they did not show any evidence of exhibiting a virgin state. The virgin state of all other CID's is manifest by an initially high threshold voltage for a device which has never been switched before. After the first switching, all subsequent switching is at a consistently lower voltage. Several experimental runs have confirmed the absence of the virgin state if metal contacts do not touch the insulating layer. Table I summarizes data taken from devices of the structure of Figs. 8(a) and 8(b). These devices had identical insulating polysilicon layers. Note that the double-layer polysilicon devices had a much narrower range of threshold voltages.

TABLE I

Threshold Voltages of Devices Made With Single and
Double Polysilicon Layers.

Device Structure	Threshold Voltage at First Switching	Threshold Voltage for Subsequent Switching
Single insulating polysilicon layer	70	10 - 20
Double polysilicon layer	14.5 - 15.5	14.5 - 15.5

C. SECONDARY PROPERTIES OF POLYSILICON CID STRUCTURES

Several aspects of the behavior of polycrystalline silicon NCL CID structures deserve further investigation because of their potential impact on the production of CID integrated circuits. Primary among these is the greater uniformity of polysilicon CID behavior, especially with regard to threshold voltage. Because variations in device design are still being explored, it is too early to conclude that the use of polysilicon is in itself a truly superior fabrication technique; however, we have observed one run in which all devices had their threshold voltages within a narrow range (15 ± 0.5 V).

This result was obtained with the double polysilicon layer devices.

A second potentially important property is that the type of collector metallization is quite immaterial. This is true for both the double and single layer polysilicon devices. Furthermore, there is some evidence that rapid transfer from insulator reactor to vacuum metallization equipment is not required for either good yield or other desirable properties (low leakage current in the high impedance state, for example). This permits greater freedom in device processing. The fact that metallization need not be applied immediately following the deposition of the insulator layer permits, in particular, the application of photoresist and insulator layer etching before metal is applied. Such a sequence of fabrication can eliminate a metallization step since base and collector metallization can be applied simultaneously.

We have also not observed the "INHIBIT" effect (to be described in detail in Sec. 10) in multiple collector devices which are fabricated from polysilicon devices. This result is viewed as preliminary since only a few multiple collector polysilicon devices have been examined. If this is generally true, then major simplifications could result in integrated circuit processing, since in emitter-base-collector memory circuits the INHIBIT function should be eliminated. (One would not desire the application of a voltage pulse to one part of the circuit to affect the switching of another device on the same chip at some later time.) Although such interactions between devices could be eliminated in principle by isolation diffusions, circuit processing could be simplified if such steps were unnecessary.

Finally, the absence of an intermediate state in the I-V characteristics of polysilicon devices could provide a greater freedom of choice in circuit design since, if present, the effect of the intermediate conductivity state can be eliminated only by proper choice of collector load resistance and voltage bias. This appraisal supposes that in its initial application the CID will be used in binary rather than ternary logic system. While such a "three-level" memory is certainly conceivable, it is not viewed as the path of earliest systems acceptance of the device.

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D. DETAILED BEHAVIOR OF EMITTER-BASE-COLLECTOR THREE-TERMINAL CID'S

Double-layer polycrystalline silicon CID structures have been fabricated with the general structure shown in Fig. 8(b) but with a heavily doped region beneath the base contact and their performance examined. These devices have produced the highest sensitivity of threshold voltage to base current drive of all devices fabricated. Figure 9 shows common emitter characteristics of one such run of devices which were of a p-type epitaxial layer grown on an n^+ epitaxial substrate. The ratio $\Delta V_{th}/\Delta I_B$ is equal to 3×10^5 ohms for these devices. The current which can be repeatably and reliably switched in the collector circuit is approximately 10^4 times the base current.

The threshold voltage of the double-layer polysilicon devices when not illuminated and with zero-base current tends to be relatively high. As would be expected with such properties, the surface depletion layer is extremely wide. Figure 10 presents the capacitance as a function of voltage for one such run which has a threshold voltage of 50 V. This device had an area of 1.07×10^{-4} cm^2, with a capacitance of 0.172 pF at 40 V bias, the depletion width at 40 V is 6.2 μ.

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I_C (0.1 mA/div.)

V_C (1 V/div.)
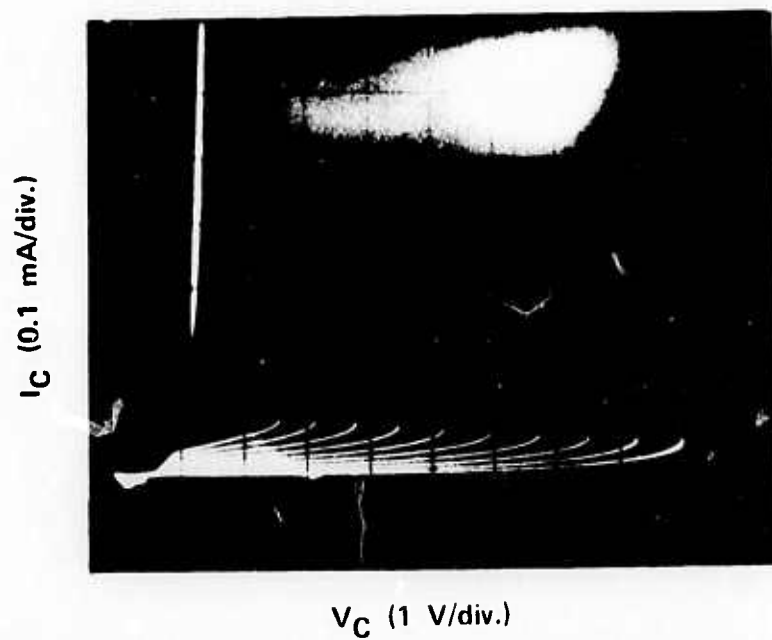
FIG. 9 Common emitter characteristics of double layer polysilicon CID structure. The various traces correspond to changes in base current increments of 2 μA. The highest threshold voltage occurs when $I_B = 0$ and the lowest when $I_B = 18$ μA.
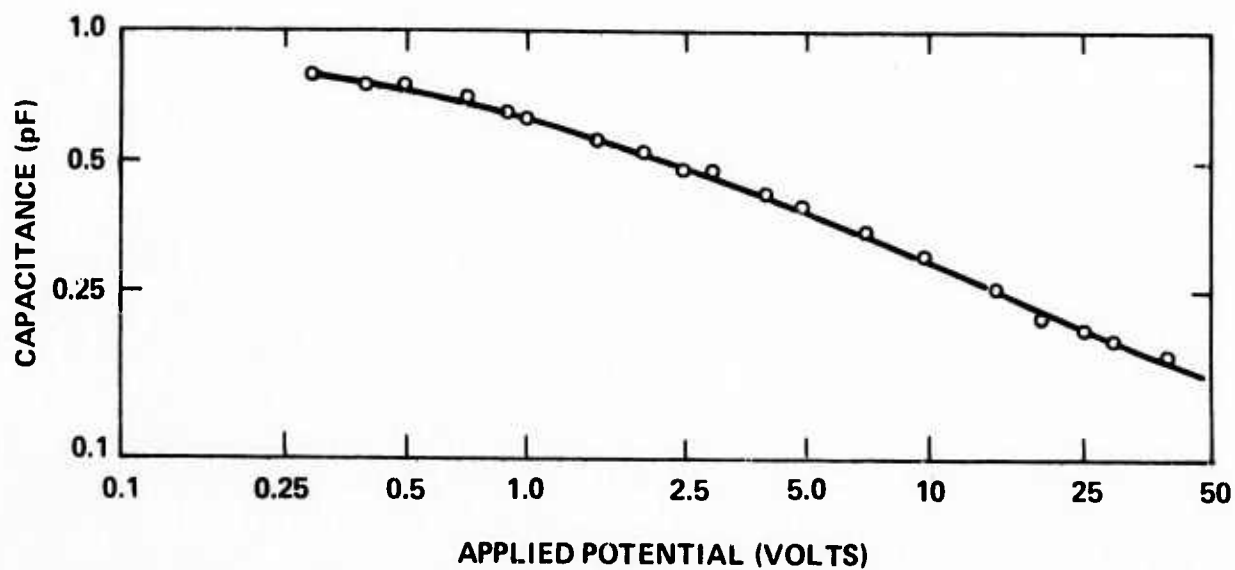
FIG. 10 Capacitance vs applied voltage of double layer polysilicon device in high
impedance state. Data taken at frequency of 1 MHz.

SECTION 4

CID STRUCTURES WITH AMORPHOUS SILICON NONLINEAR CONDUCTORS

Controlled inversion devices have been fabricated with amorphous silicon as the insulator layer. The potential advantage of amorphous silicon insulator layers arises from the fact that the deposition can be accomplished by sputtering, which is essentially a room-temperature operation, thus eliminating all high-temperature fabrication steps following epitaxial growth. Indeed, these devices have had the most consistent properties of any variation of CID structures which have been fabricated. In addition, the amorphous silicon-insulator layer devices have shown the lowest reproducible current density in the high-impedance state of any structural variation of the CID which has been fabricated to date. Besides being of utility in the fabrication of integrated circuits using CID's, the low current density of these devices has enabled convenient and accurate measurement of the capacitance of three-terminal devices under full bias conditions near the threshold voltage. Such measurements, which will be described in the next section, have been useful in confirming the basic model of the CID phenomenon.

A. STRUCTURE AND BASIC FABRICATION PROCESSES FOR AMORPHOUS SILICON INSULATOR LAYER DEVICES

The amorphous silicon insulator devices were fabricated using 150-175 Å of amorphous silicon which was applied by sputtering. (Presumably, the amorphous silicon could also have been applied by chemical vapor deposition with similar results, but sputtered layers were used for convenience and to demonstrate that low-temperature processing is sufficient for producing CID structures.) The potential utility of amorphous silicon in CID structures was first suggested almost two years before actual fabrication,[4] although the specific advantages of the material were not recognized at that time beyond the possibility of using insulator layers which were at least several hundred angstroms thick and therefore, presumably, more reproducible.

The structures fabricated using amorphous silicon are shown in Fig. 11. If base contact diffusions were used as shown in Fig. 11(c), then the
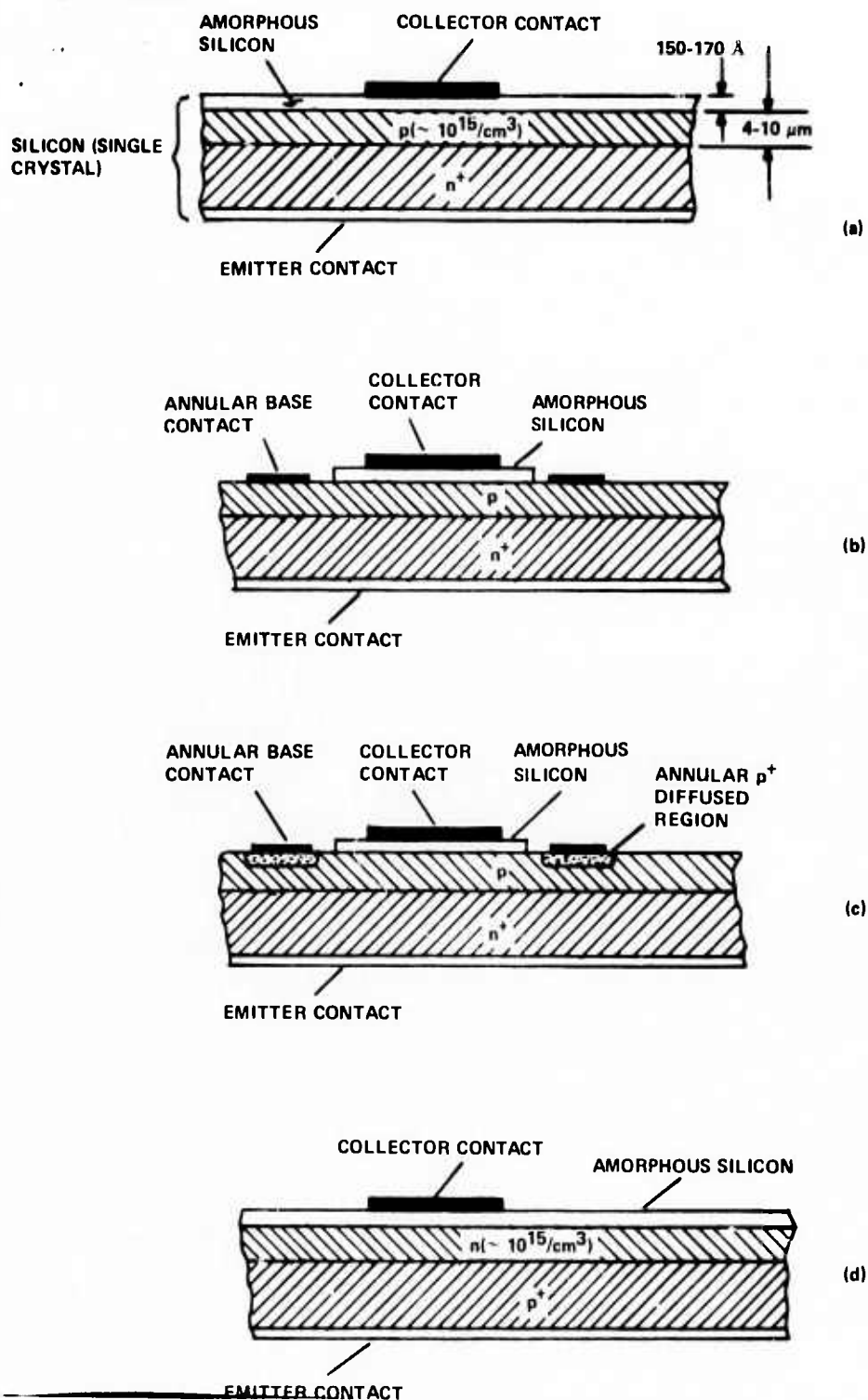
FIG. 11 Cross-sectional views of four CID structures fabricated using amorphous silicon:

(a) Metal/amorphous silicon/p/n$^+$ diode;

(b) Metal/amorphous silicon/p/n$^+$ triode;

(c) Triode with diffused base contact area;

(d) Metal/amorphous silicon/n/p$^+$ diode.

diffusion was accomplished prior to the amorphous silicon deposition. In all cases, the silicon was rf sputtered from a 6-inch diameter target using an input power of approximately 100 W. The deposition rate was 30-40 Å per minute.

It was found that it was possible to apply the base contact metal-lization either before or after the amorphous silicon layer was sputtered. If the silicon is deposited first, then it must be removed before the base metallization is applied in order to avoid making the base contact a col-lector contact of a second controlled inversion device. This structural variation is shown in Figs. 11(b) and 11(c). If the base metallization is applied first then, at least for discrete devices, it is not necessary to remove the overlying amorphous silicon layer before bonding a base contact lead to the base of the device. The thermocompression bonding process effectively breaks through the 150 Å thick silicon layer to form a mechanically rugged and electrically low-resistance contact to the underlying base metal-lization.

It appears that an evaporated layer of chromium-gold metallization over the amorphous silicon will make adequate ohmic contact to the under-lying, previously applied primary base metallization, even if mechanical disruption of the silicon layer is not obtained. This presumably occurs because any voltage applied to this contact will be applied directly across the amorphous silicon, since the sandwiching metal layers cannot support any significant voltage. The utility of this procedure for integrated circuit fabrication has not yet been confirmed, however, even though it eliminates at least an etching step and also, perhaps, a photoresist masking step. This procedure is open to question, not because it does not always work, but rather because sometimes it is necessary to pass current through the collector contact before a low-resistance connection is made.

The structure of Fig. 11(d), which shows a metal/amorphous silicon/ n-type silicon/ p^+-type silicon layered sequence was not extensively investigated, since much higher reproducibility was achieved from the M/I/p/ n^+ structure. The latter structure may also be expected to be a faster

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device, since electrons with the higher mobility are the minority carrier in the base.

B.   PERFORMANCE OF AMORPHOUS-SILICON INSULATOR DEVICES

The I-V characteristics of CID's with amorphous-silicon insulator layers are presented in Fig. 12. Figure 12(a) shows the complete current scale, which includes the low-impedance state. The sustaining voltage of the low-impedance state is less than 2 V. It is important to observe that there is only one low-impedance state. This is generally true for amorphous-silicon insulator layer devices. Another property of amorphous-silicon CID I-V characteristics is also evident in Fig. 12(a): The current rises sharply to relatively high values compared to lower voltage current values near the threshold voltage when the device is still in the high-impedance state. The negative resistance does not reduce the voltage until much higher currents than are available at low voltages are passed through the device. This I-V curve should be contrasted with the I-V curves of the polysilicon insulator layer devices shown in Fig. 9.

The reason for the seemingly high current in the upper limit of the high-impedance state has more to do with the low current density of the device at lower voltages than to an unusually large current being required to initiate the negative resistance. Figure 12(b) displays, in an expanded scale, the I-V characteristics of the same device used to obtain the data of Fig. 12(a). The current at 15 V is only 5 μA, which for this device, whose area was 1.27 x 10^{-4} cm^2, corresponds to a current density of 4 x 10^{-2} A/cm^2.

The threshold voltage for amorphous-silicon insulator devices tends to be higher for the same single-crystal silicon structure than for any other insulator material used. This property may be ultimately used to advantage in obtaining fast devices for a given threshold voltage, since a narrower base device may be used in achieving the same threshold voltage.

The amorphous silicon CID's do evidence a virgin state, however, in contrast to the double-layer polysilicon devices described previously.

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(10 mA/div)

0

(a)

(5 V/div)

0

(0.5 μA/div)

0

(b)

(2 V/div)

0
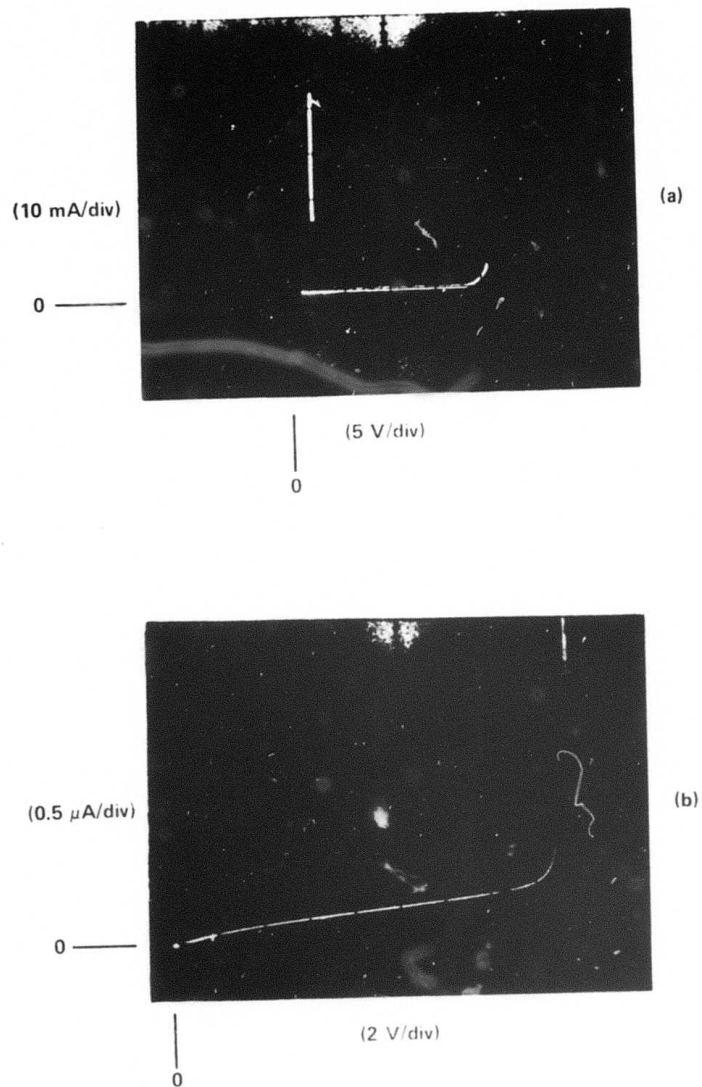
FIG. 12 Current-voltage characteristics of metal/amorphous silicon/p/n$^+$ diode;

(a) Overall I-V characteristics;

(b) Detailed i-V characteristics of high-impedance state.

The virgin state of the single-layer polysilicon devices (as for all other insulator materials) is removed with a single switching event. The collapse of the initially high threshold of the virgin state of the amorphous-silicon insulator devices to their final value is exceptional in that it is gradual. About two seconds of 120 Hz curve-tracer switching is required to produce the final equilibrium threshold voltage. It is emphasized that once produced this threshold voltage is remarkably stable, changing less than 1% over repeated cyclings with high currents. The range of final threshold voltages for various amorphous silicon devices fabricated on the same wafer is almost 10%, however. This is somewhat wider than the narrower range quoted in Table I for the double-layer polysilicon devices.

The depression of the threshold voltage by base current was not as great for the amorphous silicon insulator devices as for the polysilicon layer devices. The ratio $\Delta V_{th}/\Delta I_B$ was equal to 4×10^4 ohms for the amorphous silicon devices.

SECTION 5

MEASUREMENT OF CAPACITANCE OF CID STRUCTURES IN HIGH-IMPEDANCE
STATE UNDER ILLUMINATION AND FULL THREE-TERMINAL BIASING

One of the methods which may be used to describe experimentally the formation of the inversion layer of CID structures is obviously the measurement of its capacitance as a function of voltage in analogy with the common capacitance-voltage (C-V) measurements of standard MOS capacitors.[5] In such measurements there are difficulties present for the CID which are not present in conventional MIS devices, however. These difficulties result from the conductance of the device, which shunts its capacitive reactance. The conductance restricts the range of bias conditions under which the capacitance may be accurately measured. Furthermore, the presence of a forward-biased junction which contributes to the conduction also presents a diffusion capacitance.[6] If the contribution of the inversion layer formation to the total device capacitance is to be determined explicitly, then the effect of the CID's diffusion capacitance must also be determined.

These problems may be readily overcome for many interesting experimental situations when the device is biased into its high-impedance state (and only the formation of an incipient inversion layer is studied) by the methods described in this section of the report. Two of the interesting experimental situations are those in which the device is either under conditions of illumination or full three-terminal bias. (The capacitance of CID's in their low-impedance state will be described in the next section.)

A. MEASUREMENT TECHNIQUE AND DEVICE STRUCTURES STUDIED

The capacitance of the CID's studied was measured using a Boonton 72D capacitance meter. This instrument is capable of measuring capacitances whose Q (= ωRC) is equal to unity with a 0.1% accuracy. The measured Q's of all capacitances reported here was ≥ 2 under the conditions in which they were measured. Several precautions were found to be necessary if reproducible and precise measurements were to be taken. No electronic power

supplies were found satisfactory if three-terminal bias measurements were made, as sometimes jittery measurements resulted. The measurements were recorded by using battery supplies with potentiometers as shown in Fig. 13. Figure 13 also introduces a proposed circuit symbol for a three-terminal CID transistor with emitter-base-collector terminals. The analogy to the symbol for junction transistors is obvious. The collector terminal is different, however, and is chosen to suggest that the collector has a gate-like function besides its minority carrier collector function.

The measurement frequency was 1 MHz. Although this is an extremely high frequency for MIS capacitors, it is necessary in order to ensure that a high enough Q was obtained in order to achieve accurate capacitance measurements. For example, with $C \approx 2$ pF, if a $Q > 2$ is desired, then the differential resistance of the device (dV_{CB}/dI_C) must be greater than 1.6×10^5 ohms. The present technique will therefore no permit measurement of device capacitance if extremely high currents are passed through the collector, when dV_{CB}/dI_C will be reduced.

The present technique has also not been found to be useful if the capacitance between the emitter and collector terminals, rather than the capacitance between the base and collector terminals, is measured with full three-terminal bias conditions. This is not because repeatable measurements cannot be obtained, but rather because there appears to be no method for unambiguously nulling out the stray capacitance of the header on which the device is mounted and that of the rest of the base current supply circuit. The nulling is found to depend upon the resistance in the base current circuit. The capacitance between the emitter and collector terminals can be measured quite accurately, however, if the base terminal is left open.

The contribution of the formation of an incipient inversion layer to the CID capacitance may be readily distinguished from the contribution of a diffusion capacitance by comparing the CID's capacitance to that of a related, similarly geometrically constructed, completely bipolar device. This analogous bipolar structure is illustrated in Fig. 14, which also shows the cross-sectional view of the related CID structures. Both devices were

-27-

(a)

p-n-INSULATOR-METAL
CID

n-p-INSULATOR-METAL
CID
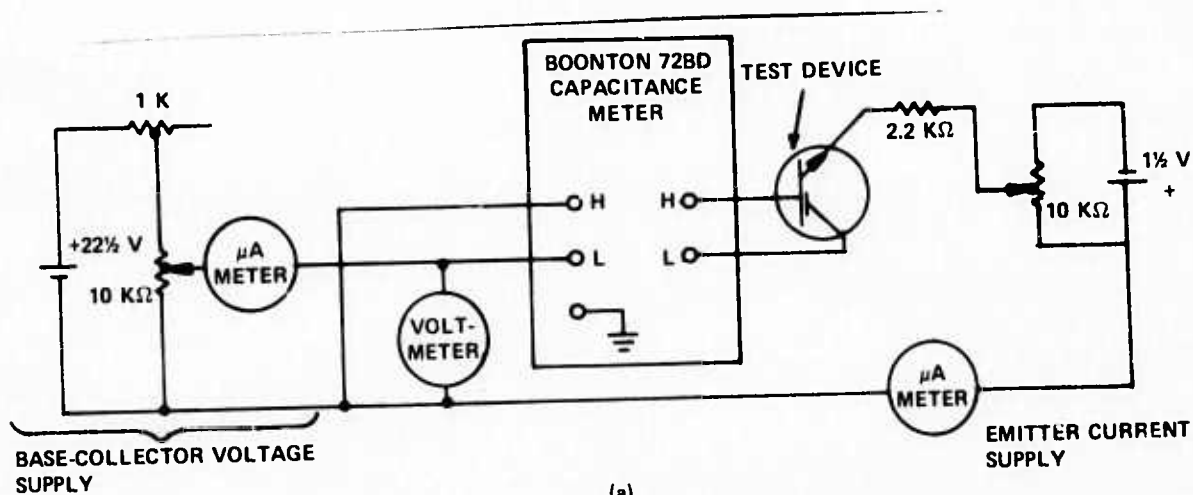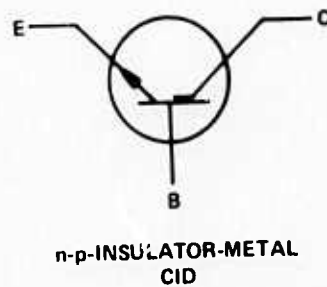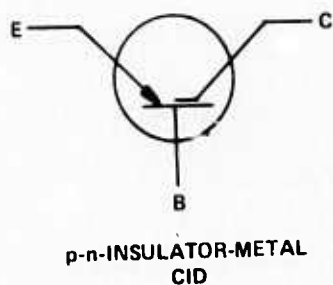
(b)

FIG. 13 (a) Experimental arrangement used to measure collector-base
capacitance when emitter current is supplied to CID.

(b) Circuit symbols for M-I-p-n and M-I-n-p CIDs.

-28-
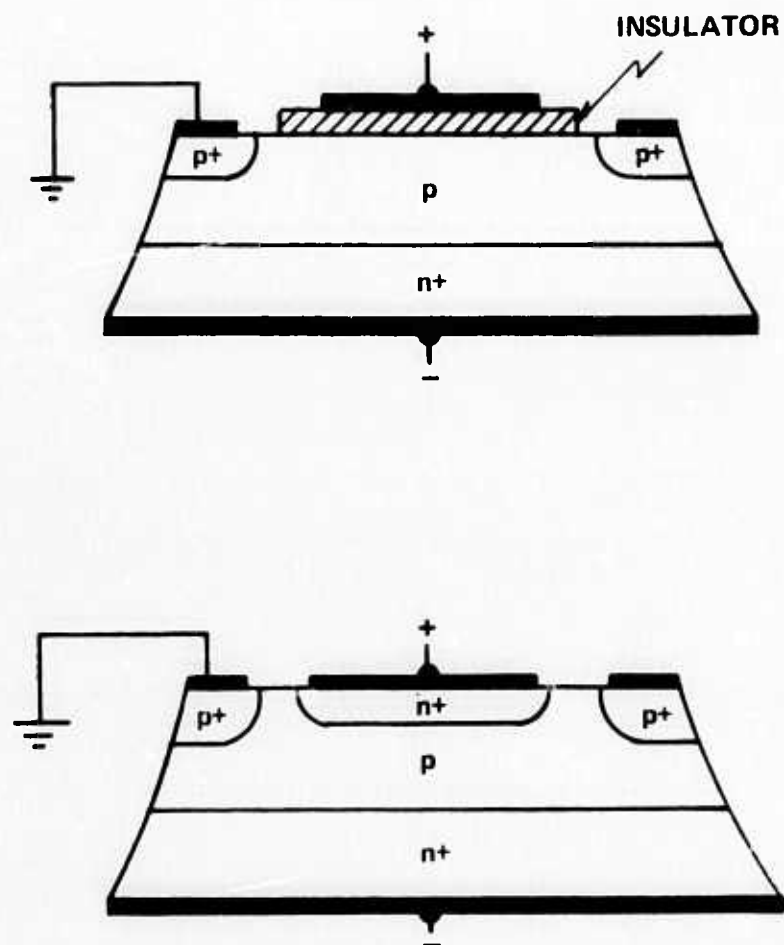
FIG. 14 Cross-sectional views of a CID structure (top) and an analogous bipolar structure (bottom). Both devices were fabricated using the same photo-resist masks. Bipolar structure cannot have contribution to its collector capacitance from inversion layer formation.

fabricated from the same silicon wafer and with the use of the same photo-resist masks.

The analogous bipolar device is essentially a transistor structure with a somewhat unusual geometric arrangement, including an emitter of large area than its collector. It is apparent that the bipolar structure can have a diffusion contribution towards its total capacitance because minority carriers will be stored in its base region if it carries current, but that no inversion layer formation is possible, since electrons will be swept into the reverse-biased collector by the electric field. Thus, differences between the capacitance of the CID and the bipolar analog under similar biasing will be due to the formation of an inversion layer in the CID.

B. EXPERIMENTAL RESULTS

Switching of a CID from one of its higher to one of its lower impedance states is possible by illumination of the device by silicon bandgap radiation. One would therefore expect that a significant increase in capacitance would occur as the radiation increases the minority carrier concentration in the base and therefore tends to form an inversion layer at lower collector biases than if no illumination were present. This is confirmed by experiment. Figure 15 displays the emitter-collector capacitance (with floating base) of an amorphous-silicon CID device as a function of emitter-collector voltage. Note that for both the illuminated and non-illuminated conditions, the capacitance tends to rise as the collector voltage increases near the threshold ($\sim$ 25 V for this particular device, which had I-V characteristics similar to those shown in Fig. 12).

The low-leakage current of CID structures made with amorphous silicon as the nonlinear conductor made these capacitance measurements possible with high accuracy. It should be noted that while the capacitance of both illuminated devices is greater than that of the same device when it is not illuminated, the capacitance of the CID in both conditions increases at high bias. This increase in capacitance is most certainly due to the incipient formation of an inversion layer. By contrast, the capacitance
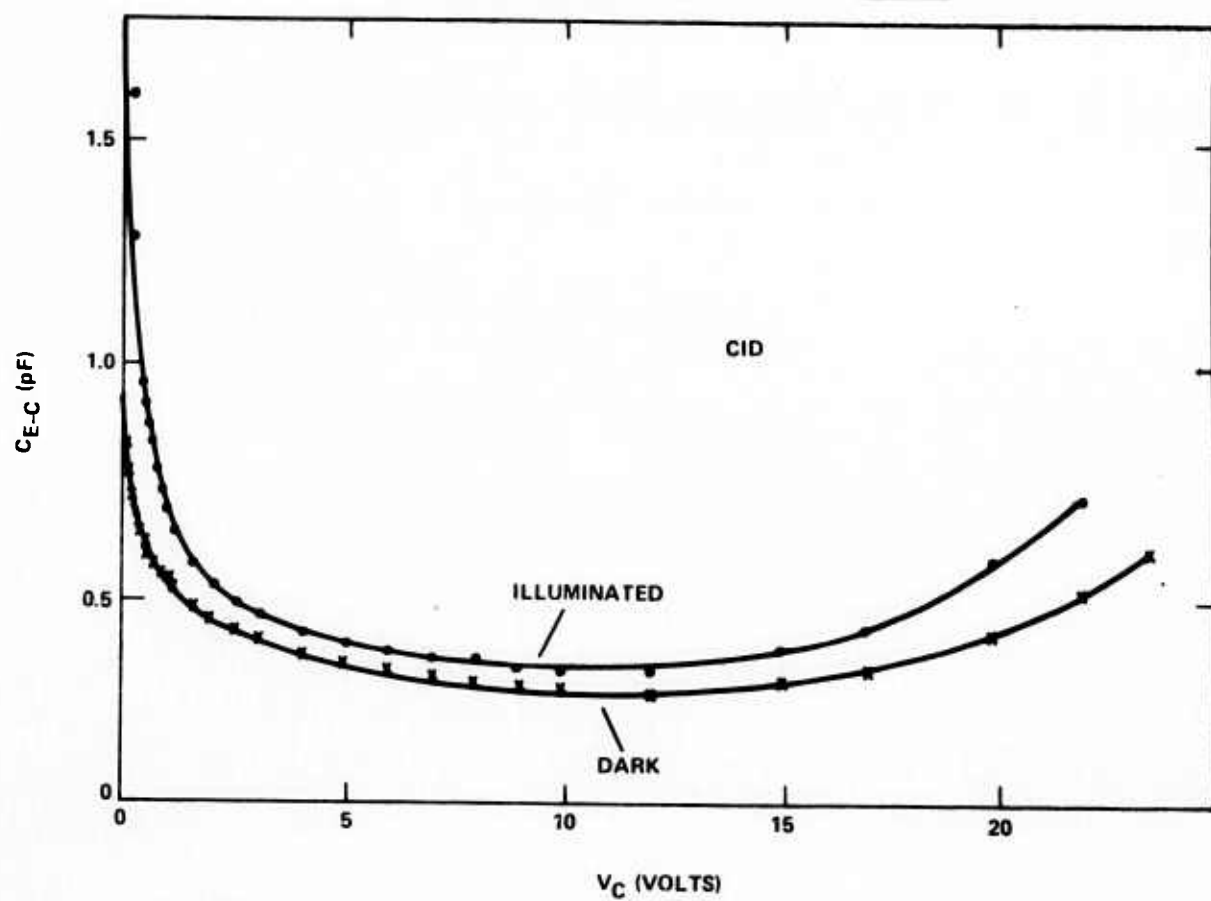
FIG. 15 Collector-emitter capacitance of amorphous silicon CID structure of Fig. 14 with floating base terminal.

between the emitter-collector terminals (with floating base) of the analogous bipolar structure is shown in Fig. 16 for conditions of no illumination and illumination identical to that used for the CID's measurements of Fig. 15. It is clear from Fig. 16 that illumination can increase the diffusion capacitance of both the CID and the bipolar device, but comparision of the data of Figs. 15 and 16 shows that the increasing capacitance of the CID at higher voltage biases is due to partial inversion layer formation. The data of the bipolar structure is shown only with the same voltage range as that of the CID whose threshold voltage was 25 V. If continued to voltages near the common-emitter breakdown voltage of the bipolar structure (above 50 V), the data would show that the bipolar device had a capacitance which was a monotonically decreasing function of reverse collector voltage for both its dark and illuminated states.

Figure 17 displays the collector capacitance of the CID whose emitter-collector capacitance was presented in Fig. 15 when the emitter terminal has been shorted to the base terminal. Note that capacitance of the device under these conditions does not increase at higher collector voltages, and is not particularly sensitive to illumination. This is a reasonable result because both the diffusion capacitance and inversion-layer capacitance will be reduced because of reduced minority-carrier injection when the emitter is shorted to the base. The dark capacitance is also shown on a contrasted scale for forward biasing of the collector-base contact. The capacitance in this case approaches the capacitance of the insulator layer. If the emitter-collector capacitance with floating base were measured, then the capacitance would decrease sharply with forward biasing of the collector, as this sense of bias would also imply that a reverse bias was applied to the emitter junction which is in series with the collector. Thus the capacitance of the insulator would not be directly observed if the base were floating.

Figures 18 and 19 present data on the collector-base capacitance of the CID when emitter current is supplied to the device. The collector-base capacitance as a function of collector voltage is shown in Fig. 18 with the emitter current I_E, appearing as a parameter. When $I_E = 0$, then the
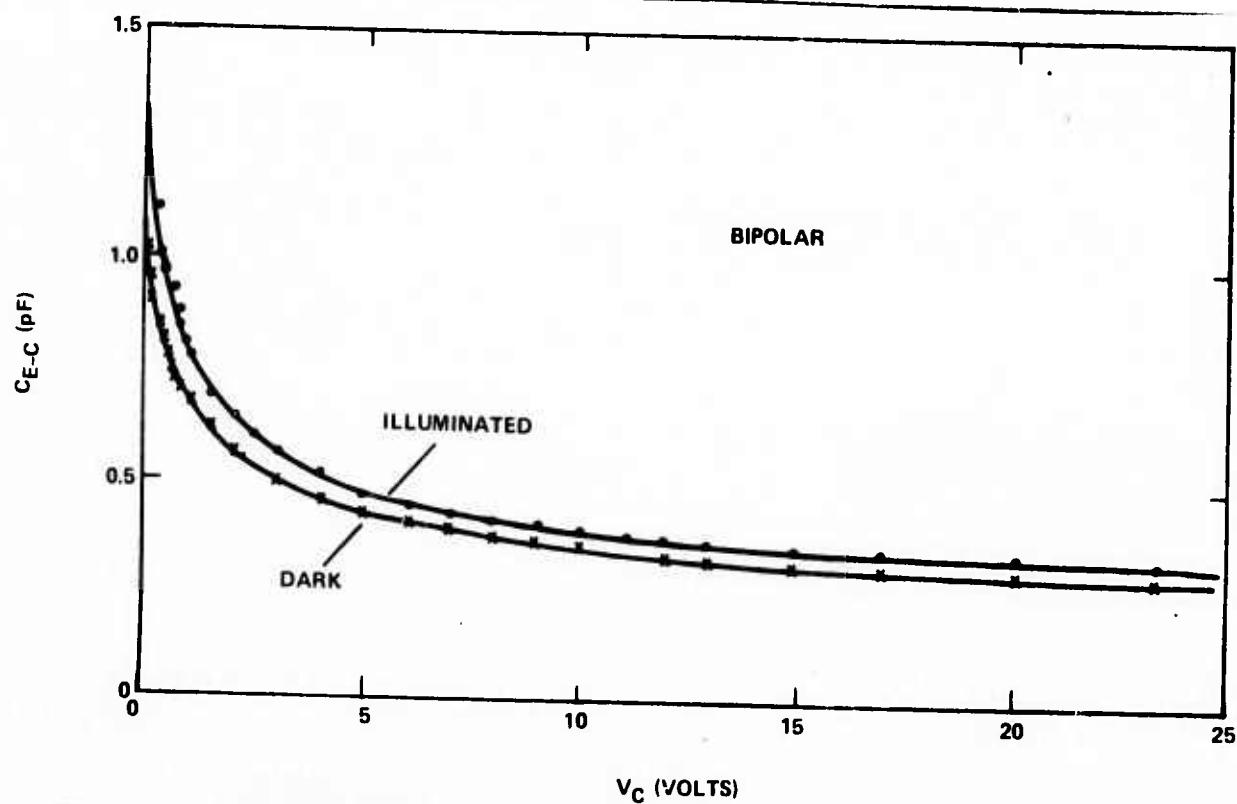
FIG. 16 Collector-emitter capacitance of analogous bipolar structure of Fig. 14 with floating base terminal.
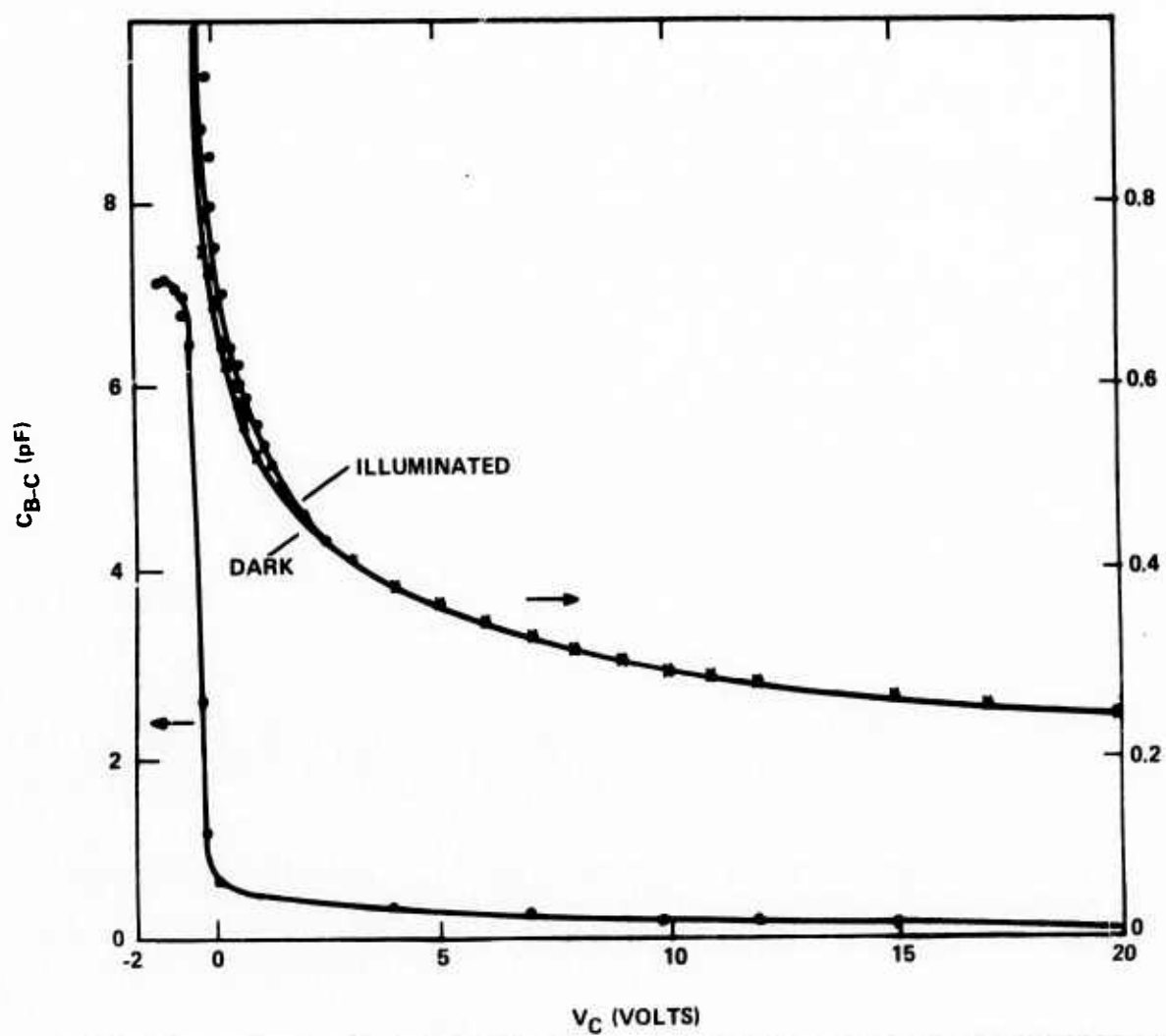
FIG. 17 Collector-base capacitance of amorphous silicon CID structure with emitter shorted to base.
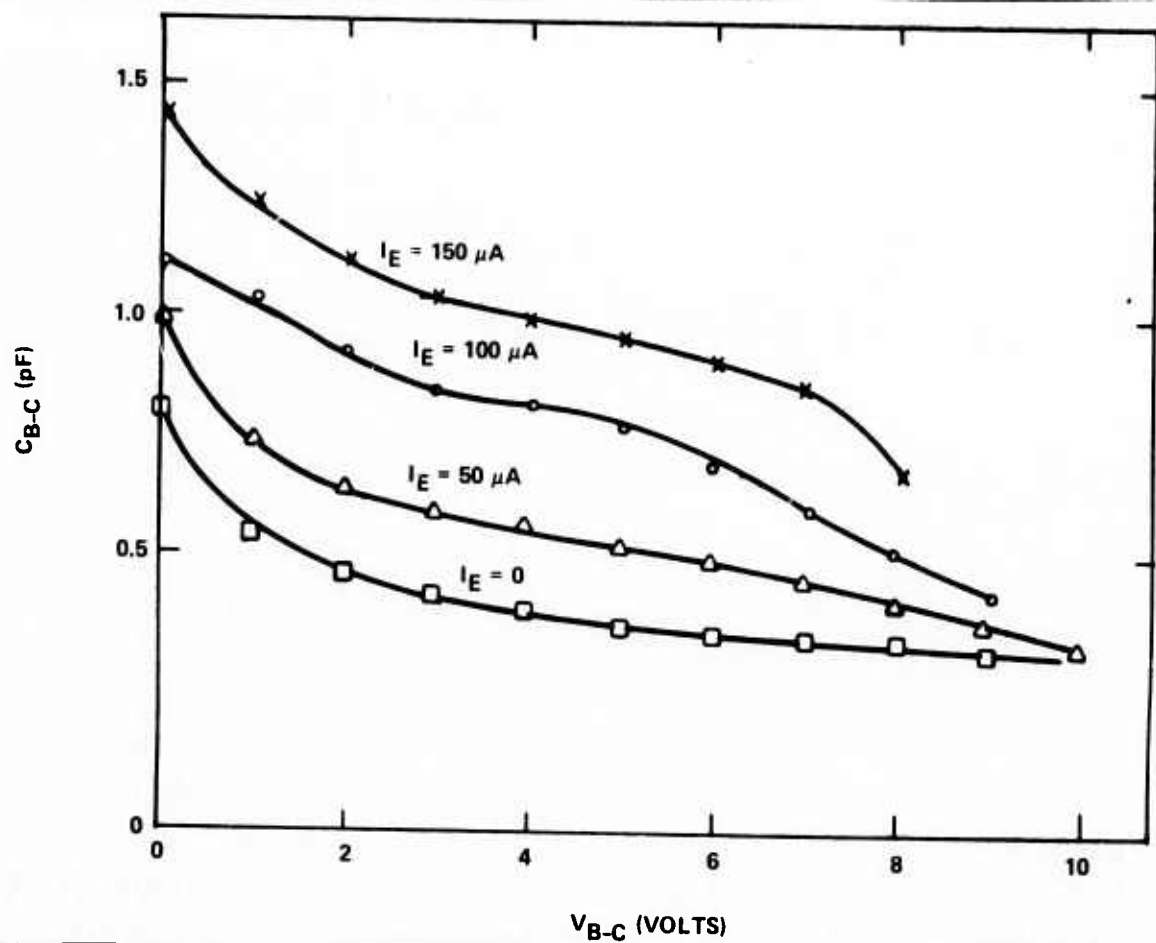
FIG. 18   Collector-base capacitance of three-terminal amorphous silicon CID as a function of collector-base coltage.   Different curves correspond to different emitter currents as labeled.
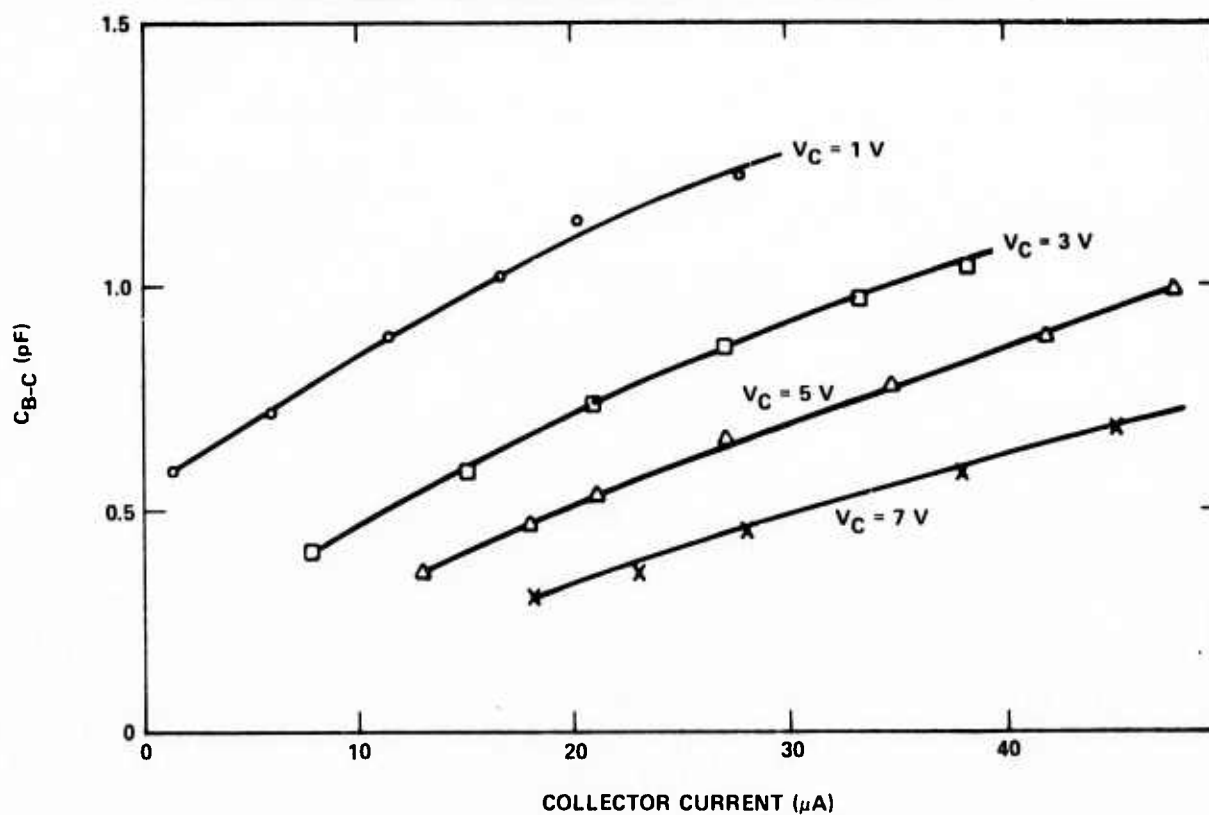
FIG. 19 Collector-base capacitance of three-terminal amorphous silicon CID as a function of emitter current. Different curves correspond to different base-collector voltages as labeled.

results are essentially the same as for Fig. 17. Increasing the emitter
current raises the collector capacitance at low voltages. This change is
much greater for the CID than for the analogous bipolar structure. At higher
collector voltages the difference between the curves for different I_E
decreases. This is because the higher collector-base voltages imply a
greater conductance of the nonlinear conductor, which therefore causes a
dissipation of the incipient inversion layer formed by the minority carriers
injected into the base from the emitter. Data at higher collector voltages
could not be obtained because of deterioration in device Q. Figure 19 dis-
plays data on the capacitance as a function of emitter current with base-
collector voltage as a parameter. If collector-emitter terminal capacitance
could be measured, with base current as a parameter, one would not expect a
reduction in capacitance at higher collector-emitter voltages.

SECTION 6

CAPACITANCE MEASUREMENTS ON DEVICES IN HIGH CONDUCTIVITY STATE

A. PURPOSE AND METHOD

Measurements of the capacitance of semiconductor devices yield valuable information about the internal parameters of the device: width of a depletion layer, or amount of stored charge in neutral layers. Such information would be desirable to have for the CID. However, in the high conductivity states the device's capacitance is shunted by a relatively high conductance and this severely limits the accuracy of the measurements of the capacitance. One method of securing the capacitance data is to work at much higher frequencies in the microwave band where the capacitive impedance can become comparable to the resistance.

This method of measuring CID capacitance has been used. The data agrees with 1 MHz measurements for the capacitance in the high impedance state and have provided the first measurement of capacitance of CID's in their low impedance states. The method consists of mounting a CID in a microwave varactor package and placing the package at the termination of a 50 Ω coaxial transmission line. The reactance of this complex circuit is measured at $\sim$ 1 GHz using an HP network analyzer. The capacitance of the chip can be inferred from this measurement.

The means of making this inference are probably worth describing, since they are likely to be familiar only to those readers who have specifically microwave semiconductor experience. The equivalent circuit of the packaged diode terminating a coaxial line is shown in Fig. 20. In this figure, the terminals A-A' represent the impedance seen in the coaxial circuit just at the point where the packaged diode is mounted.

The circuit element C_1, C_2 and L_{RM} represent the net effect of the impedance caused by a transition from the coaxial line to a radial mode cavity formed by the end wall of the coaxial circuit, the outer conductor, and the end of the center coaxial conductor.[7] These impedances are somewhat affected

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COAXIAL MODE TO
RADIAL MODE TRANSITION

MODEL OF
ACTUAL DEVICE
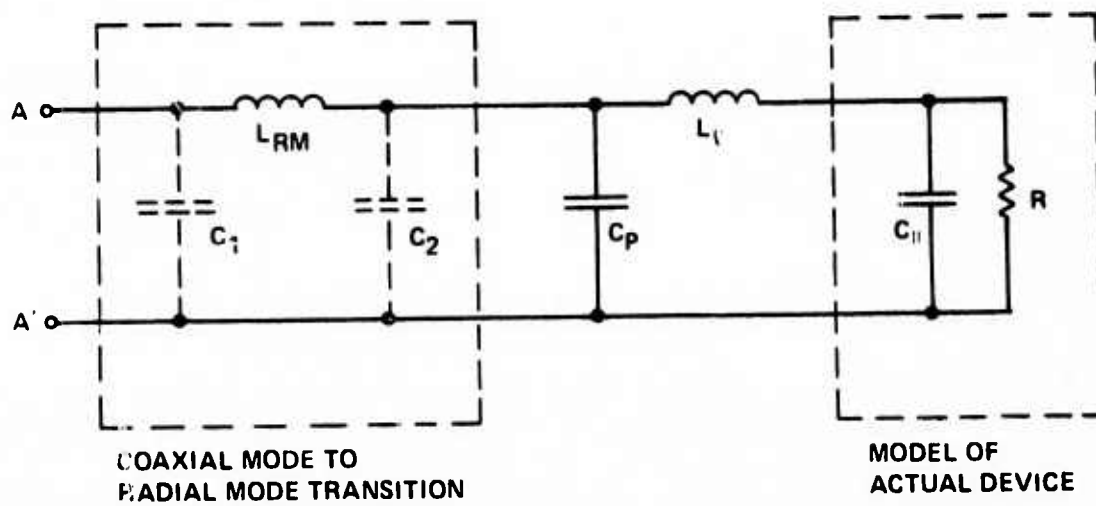
FIG. 20   Equivalent microwave circuit of package diode mounted in termination
of coaxial transmission line.

by package size, but are mainly dependent on coaxial line dimensions. For the particular package and coaxial line used, C_1 and C_2 are small enough to be negligible and the radial mode inductance $L_{RM} = 0.4$ nH. The capacitance of the varactor package C_p was 0.15 pF and the inductance L_ℓ which was 0.4 nH is produced by the wire leads which connect the chip to the lip of the package. With the knowledge of these circuit elements it is possible to calculate the effective parallel capacitance C_{11} and resistance R of the active diode from measurements of the impedance seen at terminals A-A′.

B. MEASUREMENTS OF NARROW BASE DEVICES AT LOW MICROWAVE FREQUENCIES

The first measurements made are presented in Fig. 21 for devices of the type diagrammed in Fig. 3 when they were biased into the low-impedance states. These devices were of relatively narrow base width[6] (less than 5 μm). The capacitance is seen to increase with larger currents, which is suggestive of a diffusion capacitance. In fact, one might expect[12] that the measured capacitance C should be given by

$$C = C_{d\ell} + C_d \tag{4}$$

where $C_{d\ell}$ is the depletion layer capacitance of the surface depletion zone corrected by any ability of an inversion layer to follow the signal, and C_d is the diffusion capacitance of the base region. According to simple theory,[6] for low frequencies

$$C_d = \frac{IW_B}{D} \frac{\partial W_B}{\partial V_C} \tag{5}$$

where I is the applied current, D is the diffusion constant for the minority carriers in the base, W_B is the width of the neutral base region and V_C is the collector voltage.

Note that Eqs. (4) and (5) are quite obviously appropriate for providing at least a qualitative explanation for the date of Fig. 21. In
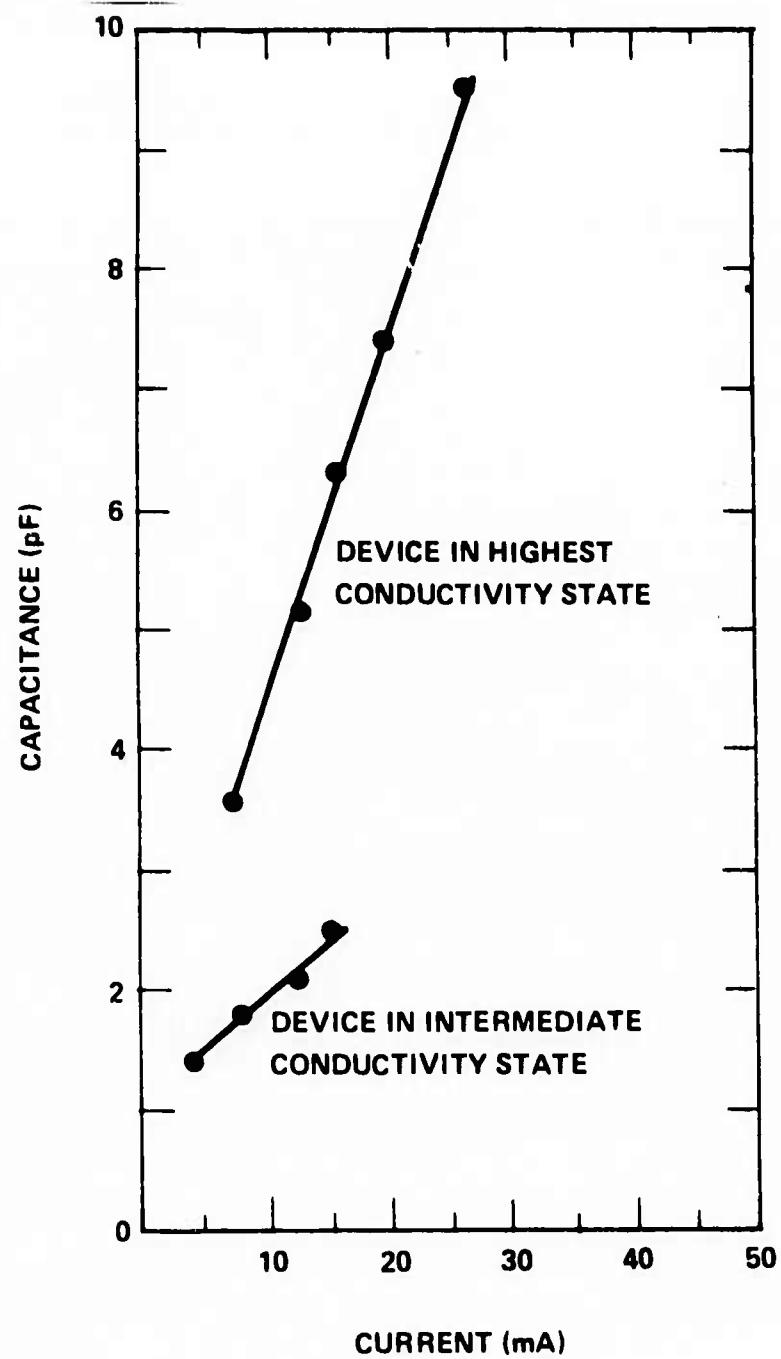
FIG. 21 Graph of capacitance measured at 1 GHz vs current of CID device diagrammed in Fig. 3 with open base connection.

particular, the I = 0 intercept of the curves does in fact yield the capacitance of the device at that same voltage but in the high-impedance state. Second, an approximately linear dependence of C on I is observed. Finally, one may note that the slope of the curves for two impedance states are consistent with Eq. (5) and the fact the lowest impedance state has the lowest voltage. The lower voltage implies a narrower surface depletion zone and therefore a greater width W_B of the base region. According to Eq. (5), a plot of C vs I should have a greater slope for a wider neutral base region.

There remains a question as to the value of $\partial W_B / \partial V_C$ which should be used in Eq. (5), however. In the high-impedance state, $\partial W_B / \partial V_C$ appears to have almost exactly the value that would be found if a Schottky-barrier contact, instead of the metal nonlinear conductor contact, were used. In the low impedance states it is not clear that the simple electrostatic arguments on the width of a depletion zone apply to a CID. If we were dealing with a simple MIS structure, we could safely assume that at tne 1 GHz measurement frequency that the surface inversion layer could not follow the voltage variations applied to the metal contact,[11] but with the CID, which has a ready supply of minority carriers, the surface depletion zone might well be able to follow the applied signal.

Initial analysis of the data will be made under the assumption that the inversion layer cannot follow the high-frequency variations. If this is the case, we may evaluate $\partial W_B / \partial V_C$ by assuming that all of the extra voltage applied to the collector will be developed in the surface depletion layer. Therefore, $\partial W_B / \partial V_C = - \partial W_S / \partial V_C$, where W_S is the width of the surface depletion layer. For the structure studied in Fig. 3, with uniform doping of the semiconductor near its surface,

$$\frac{\partial W_S}{\partial V_C} = - \frac{W_S}{2V_C} \quad .$$

-42-

For the lowest impedance state $V_C \approx 2$ V and $W_S \approx 1.6$ μm. Further, if we take $D \approx 40$ cm^2/s for electrons, we find from Eqs. (4) and (5) that

$$\frac{\partial C}{\partial I} = \frac{W_B}{D} \frac{\partial W_B}{\partial V_C} = \frac{1.4 \times 10^{-4}}{40} \frac{1.6 \times 10^{-4}}{2 \times 2} = 1.4 \times 10^{-10} \text{ F/A} = 0.14 \text{ pF/mA} \quad , \quad (6)$$

where we have taken W_B to be the difference between the depth of junction below the surface (3 μm) and the calculated value of W_S (1.6 μm).

The slope of the C vs I curve of Fig. 21 is about 0.4 pF/mA. One reason for the difference could be that the method of calculation $\partial W_B/\partial V_S$ is not valid because the inversion layer can respond to the 1 GHz measurement frequency. Some support for this reasoning is given by measurements of the capacitance of the device type shown in Fig. 4 when biased into the intermediate impedance state. These measurements are presented in Fig. 22. The measured values of $\partial C/\partial I$ at small values of current are about 1 pF/mA, and the value calculated from Eq. (1) is 1.2 pF/mA. The device used for this measurement had a considerably wider epitaxial layer than did the device from which the data of Fig. 21 were obtained. The surface depletion layer had a width of 3.2 μm in the intermediate state and the neutral base region was about 6 μm. The greater base width of this device could tend to prevent the surface depletion layer from rapidly following the applied field, thus making the device more nearly conform to the assumption made above that the inversion layer cannot follow high-frequency variations at all.

The frequency dependence of C_d,[6] which tends to reduce C_d at high frequencies, has not been taken into account. If standard expressions for the frequency dependence of C_d are directly applicable to the CID structure, then a further descripancy results as the calculated values of C_d would differ even more from the measured values.
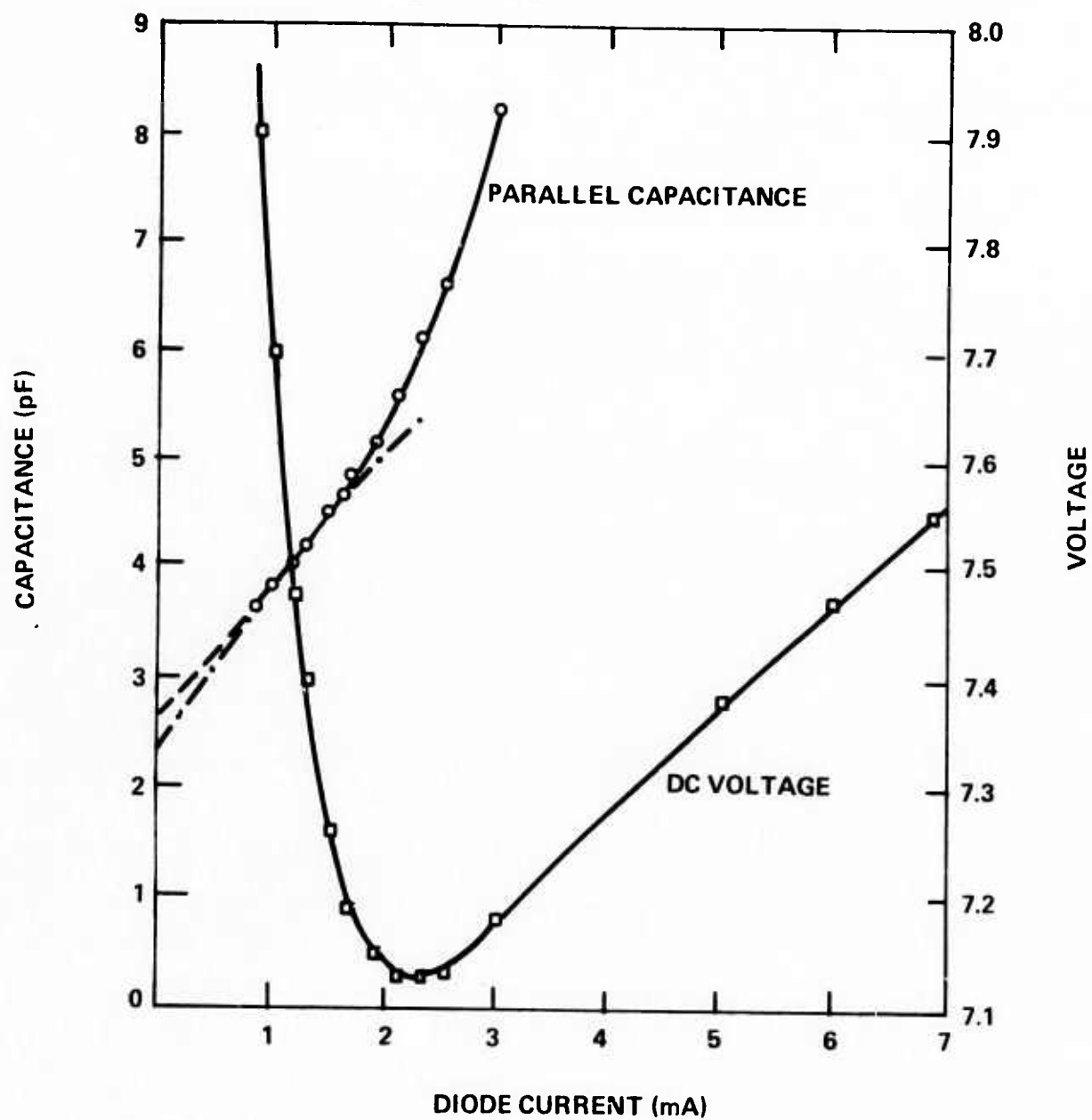
FIG. 22 Graph of capacitance measured at 1 GHz vs current of CID diagrammed in Fig. 4 with open base connection. Device is biased to intermediate-level impedance state.

C. MEASUREMENTS OF WIDE BASE DEVICES AND NARROW BASE DEVICES AT HIGHER
   MICROWAVE FREQUENCIES

The method of disembedding the impedance of a diode from its pack-
aging reactances and circuit mounting reactances will lose accuracy if the
device itself can react with other circuit elements to form resonant circuits.
With high currents and at higher microwave frequencies, the devices whose
measurements were reported in the previous section do form resonant circuits
with other mounting elements. The reactances of these devices cannot be
measured with the same accuracy as at lower frequencies. However, it is
qualitatively clear that the reactance of the devices at 10 GHz differs even
more in the low-impedance state from the high-impedance state than it does
at 1 GHz. The devices evidenced extremely high capacitances (50 - 100 pF) or
even had inductive reactances in the 5-10 GHz band.

An attempt to understand the reasons for this was made by examin-
ing extremely wide base ($\sim$ 10 μm) devices at lower frequencies. Figure 23
shows a Smith Chart plot of the impedance of an amorphous silicon CID with a
9.5 μm base width made at 1 and 2 GHz as a function of dc bias. The lower
half of the Smith Chart shows capacitive reactance and the upper half shows
inductive reactance; points lying near the perimeter of the circle show
higher magnitude reflection coefficients than points lying nearer the center
of the chart which represent better matches to the 50 Ω line. A short cir-
cuit appears as a point on the left-hand edge of the chart (impedance = 0
and angle = 180°); as open circuit appears as a point on the right-hand edge
of the chart (impedance = ∞ and angle = 0°).

At zero bias the impedance of the device is in the lower right-hand
quadrant with significant loss. As the bias increases the loss decreases,
and near threshold the device is a nearly pure capacitive impedance. As the
dc current increases near V_{th} the device again becomes lossy while its
capacitance continues to decrease. The impedance jumps to the upper left-
hand quadrant when the low-impedance state is obtained, indicating an
inductive reactance and low resistance. Increasing the current in the low-
impedance state causes the device to become less lossy by reducing the

-45-

(a)
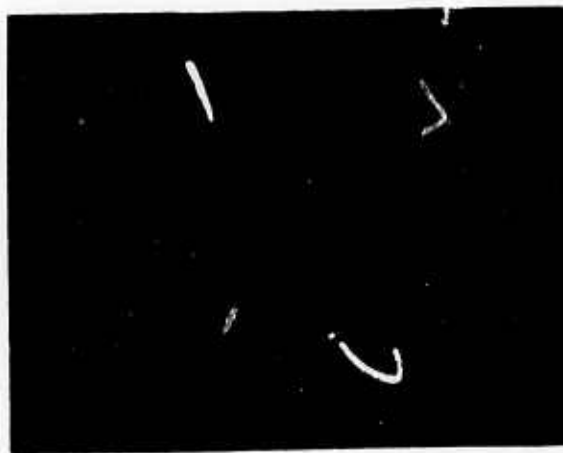
(b)

FIG. 23 Smith chart representation of impedance of amorphous silicon CID with
9.5 μm base width measured at 1 GHz (a) and 2 GHz (b) as a function
of applied bias. The device shows capacitive reactance in the high-
impedance state and inductive reactance in the low-impedance state.
The device has a minimum loss when either high voltage is applied to
the device in the high-impedance state or high current is applied to the
device in the low-impedance state.

resistance of the device to values far below 50 Ω. The peak currents shown
are 35 mA. For currents > 50 mA, the resistive component of the device was
so low it could not be accurately measured from this type of plot without
further recalibration.

Figure 24 displays the impedance of the device at two particular
bias conditions when the test frequency is swept from 1-2 GHz. The two bias
points are in the high-impedance state near threshold (which produces the
trace in the lower right-hand quadrant) and at 25 mA current in the high-
impedance state (which produces the trace in the upper left-hand quadrant.
For both high- and low-impedance states the 1 GHz data points lie near the
horizontal axis of the Smith Chart.

The precise mechanisms for the appearance of an inductive reactance
rather than a capacitive reactance in the low-impedance state have not been
established. It could involve transit-time effects as well as a suppression
of diffusive capacitive contributions by high frequency, wide neutral base
layer width effects.

D. SIGNIFICANCE OF MICROWAVE FREQUENCY IMPEDANCE MEASUREMENTS

One of the anticipated benefits of a CID memory, which was dis-
cussed in the proposal to our current ARPA program, was its potentially high
speed. In that proposal, data were presented which showed that impedance-
state transitions could take place at least as fast as 1 ns. A second feature
which must be present if an integrated array is to function as an extremely
fast memory (or as a fast crossbar switch) is that the device be capable of
being "read" within nanosecond time intervals for memory applications (or
transmit subnanosecond pulses reliably in its dc low-impedance state for
crossbar switching). These later requirements are equivalent to demanding
that the impedance of the device be very different when measured at micro-
wave frequencies in its high and low dc impedance states. The data supplied
in Sec. 6 demonstrate that this is, in fact, the case.
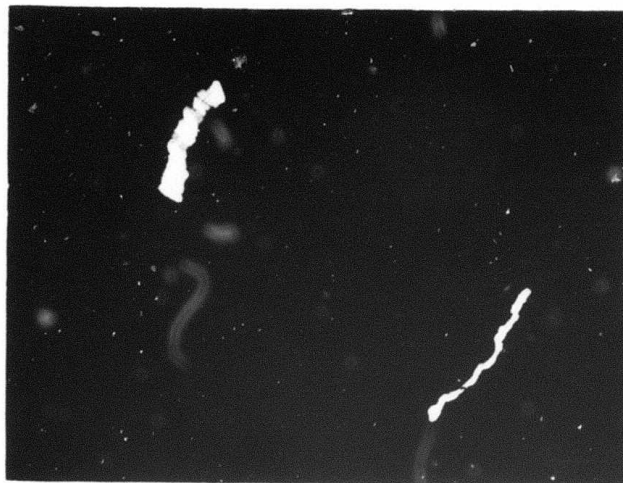
FIG. 24 Smith chart representation as a function of frequency between 1 and 2 GHz for two particular biases: device in high-impedance state with $V \leqslant V_{TH}$ and device in low-impedance state with $I = 25$ mA. In both the high- and low-impedance states the impedance points are closer to the horizontal axis at 1 GHz.

SECTION 7

EMITTER-BASE-COLLECTOR DEVICES USED AS AN AID TO UNDERSTAND CID MECHANISMS

A. COMMON BASE CHARACTERISTICS

Devices biased in the common-base mode are often unstable and can be easily damaged. Nevertheless, the study of the common-base current-voltage characteristics can provide some insight into the operation of the CID phenomenon. Typical common-base characteristics of the device diagrammed in Fig. 4, which has a silicon-rich silicon nitride as the insulator, are illustrated in Fig. 25, and the common-base characteristics of the device diagrammed in Fig. 8, which has a polysilicon insulator layer, are shown in Fig. 26.

For small collector voltages, it is seen that the collector current I_C is less than the emitter current I_E for both structures. This is generally true for all CID's. At sufficiently high collector voltage, $I_C > I_E$. This is in strong contrast to the case of normal bipolar transistors, where the magnitude of the emitter current is always greater than that of the collector current. The usual small difference, $I_E - I_B$ = base current, is interpreted as recombination current. If $E_E < I_C$, we would naturally interpret I_B as _generation_ rather than recombination current.

The collector voltage at which $I_C = I_E$ is at, or at least near, the point where the characteristics become very steep and a rapid jump in collector current occurs. These critical collector voltages are approximately equal to the collector voltages at which transitions to the low-impedance state occur in the grounded-emitter configuration (for the same collector current), as illustrated in Figs. 5 and 9. Thus, we have a strong suggestion that additional carrier generation occurs in the collector side of the device at the threshold voltage or in the low-impedance state.

It is difficult on the basis of present experiments to be certain which of several mechanisms is responsible for the excess generation. It is not likely to be primarily avalanching. The avalanche breakdown of the

-49-

I → (0.2 mA/div.)

V → (2 V/div.)
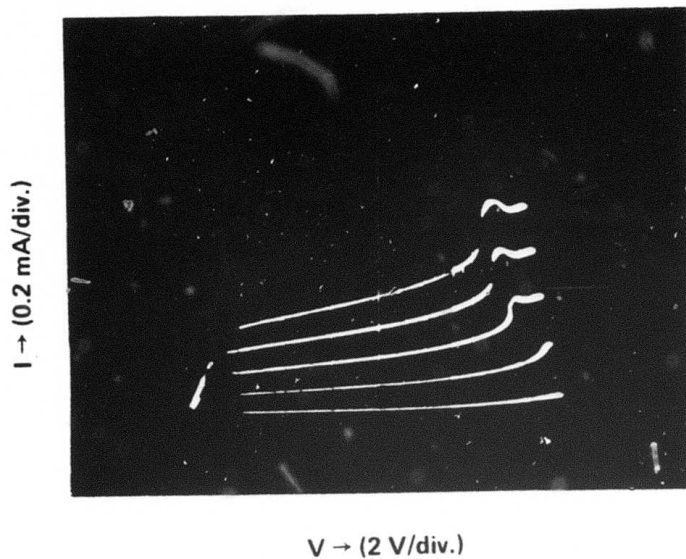
FIG. 25 Grounded base collector characteristics for devices diagrammed in Fig. 4. Curves correspond to emitter currents of 0, 0.2, 0.4 and 0.6 mA, with higher emitter currents resulting in higher collector currents.

I_C (100 μA/div.)

V_C (1 V/div.)
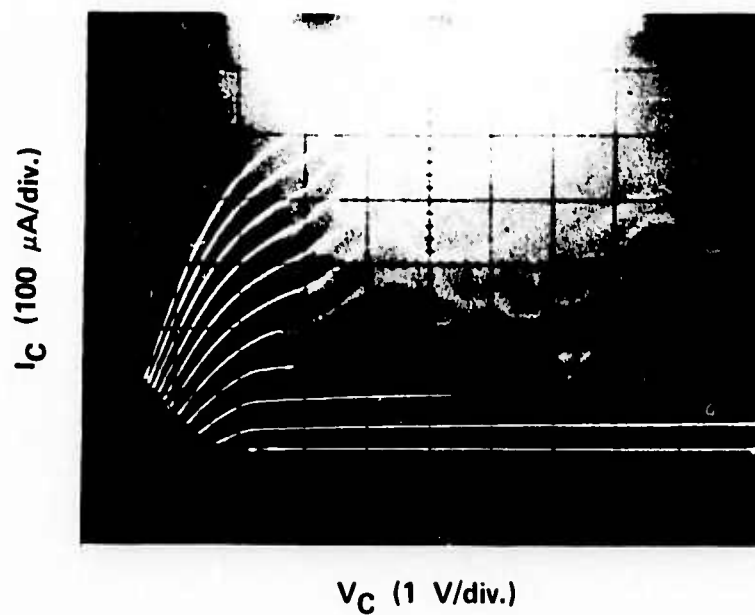
FIG. 26 Grounded base collector characteristics for double layer polysilicon device diagrammed in Fig. 5. Curves correspond to emitter currents of 0, 50, 100, ..., 500 μA with higher emitter currents resulting in higher collector currents. Note oscillation when $I_E \approx I_C$.

surface depletion zone of the devices is well beyond 150 V. It is unreasonable to assume that multiplication will exceed unity by as much as one percent at voltages in the range of 10-18 V. Another possible mechanism for generation is multiplication by carrier conduction processes at the insulator-semiconductor interface. This speculation is basically a generalization of the multiplication process described by Shewchun et al.[8,9] Shewchun has considered the particular case of tunneling of carriers completely through the insulator, an obvious impossibility in our case where the insulator is 300 Å thick. However, it is possible that carrier injection into the insulator is partially governed by tunneling processes. Finally, one might consider the possibility that carriers entering the semiconductor from the insulator (in this case holes) have sufficient energy in the valance band of the semiconductor to cause an ionization event producing an electron-hole pair in addition to the primary hole. Further investigation of these observations is likely to be crucial for developing a complete quantitative theory of the CID.

The common-base characteristics of the polysilicon CID for relatively high values of emitter current are illustrated in Fig. 27. The steep rise in collector current, which is shown in the upper part of the picture, corresponds to a device in the common-emitter configuration being in the low-impedance state. For such conditions there is a fully developed inversion layer at the polysilicon-silicon interface. The differential conductivity of the device therefore represents the differential conductivity of the polysilicon layer under conditions on an n-type silicon layer.

B. "INVERTED BIASING" OF EMITTER-BASE-COLLECTOR DEVICES

The least well-understood part of the CID structure is, of course, the thin insulator layer. Very little direct experimental evidence exists which defines the fraction of total insulator conduction current which is carried by electrons and holes. The CID structure offers one means of supplying such information if its bias is inverted.

By "inverted bias" we mean that the metal collector of the CID is used as an emitter and the p-n junction emitter is used as a collector.

-52-

I_C (0.5 mA/div.)

V_C (1 V/div.)
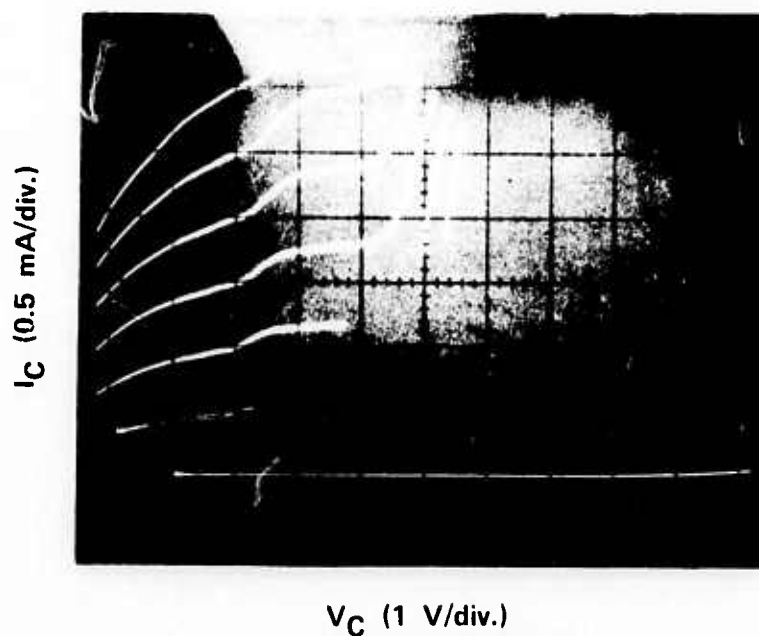
FIG. 27 Grounded base characteristics of double layer polysilicon device
diagrammed in Fig. 8(b). Curves correspond to emitter currents
of 0, 0.5, 1.0, ..., 3.0 mA. Note discontinuity in curves for
I_E = 0.5 and 1.0 mA.

-53-

This is illustrated in Fig. 28. If such biasing is applied, then the reverse-biased p-n junction should be able to sweep up minority carriers (electrons for the device type illustrated in Fig. 28) injected into the base region of the device from the metal-insulator contact. The ratio of the current I_C crossing the reverse-biased p-n junction to the current supplied to the metal contact I_E should provide (assuming good lifetime and favorable bipolar transistor geometries) a measurement of the fraction of the insulator current that is carried by minority carriers of the base region of the device.

It is recognized that while this information may be interesting, it will not necessarily be definitive concerning CID behavior. This is because the insulator has the opposite bias in this experiment than it does in CID operation. Thus, for example, differences in work function between semiconductor and metal, and the presence of either accumulation, depletion or inversion layers on the semiconductor surface could cause an asymmetry in the two directions of current transport.

All the structures which were fabricated were studied under inverted biasing. The thicker nitride structure of Fig. 4 (300 Å of silicon-rich silicon nitride) was studied more extensively because a priori it was felt that the dominant carrier should most certainly be electrons rather than holes. The data of Fig. 29, which shows the ratio of I_C/I_E as a function if I_E for the inverted bias arrangement, cannot be interpreted, however, in any obvious manner except to show that the dominant carriers in the insulator are holes.

If electrons were the dominant carrier and no complications due to an active insulator-semiconductor interface (caused by recombination, for example) were present, one would expect $I_C/I_E \approx 1$. The maximum value of I_C/I_E is about one-third according to Fig. 29. The fall-off of I_C/I_E at high emitter currents is not a property of the insulator but a property of the semiconductor geometry. This will be discussed in the next section of this report. The flat portion of I_C/I_E vs I_E and the values of I_C/I_E at low I_E do reflect properties of the insulator and/or insulator-semiconductor interface.

-54-
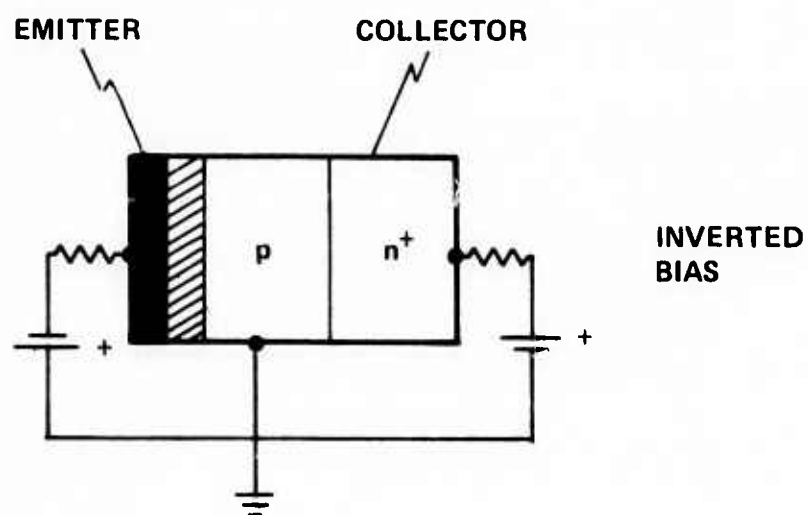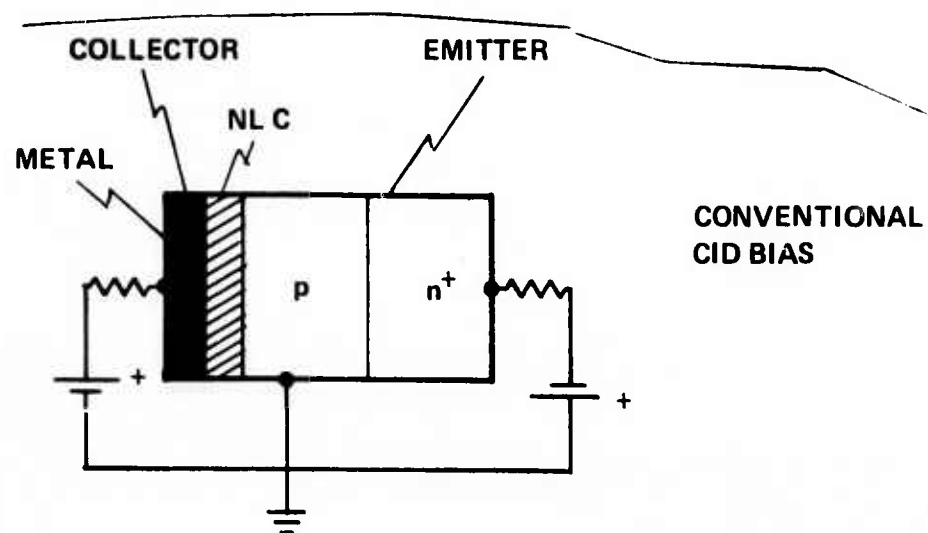
FIG. 28 Illustration of conventional and inverted biasing of CID whose structure is metal-insulator-p-n$^+$.
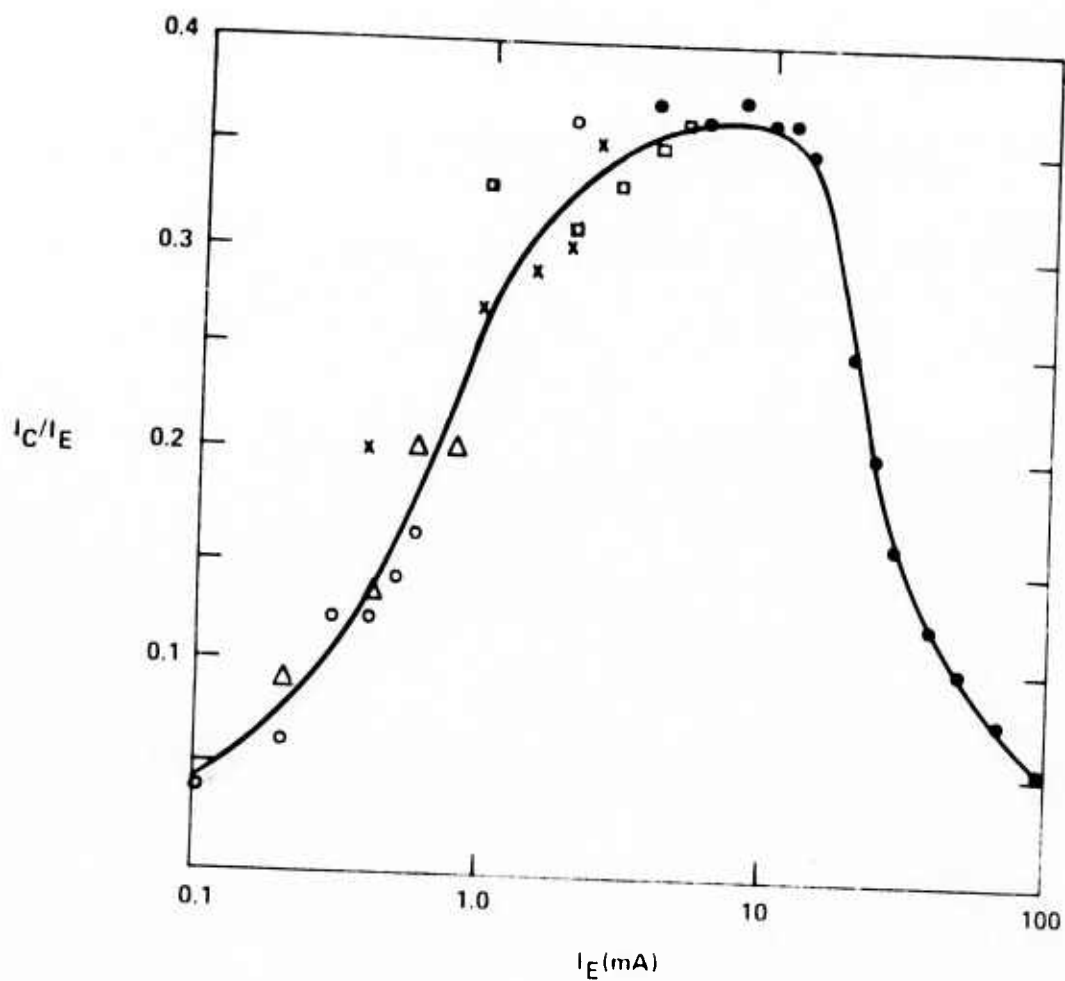
FIG. 29 I_C/I_E vs I_E for device diagrammed in Fig. 4, under conditions of inverted bias with grounded base. Here the metal contact on the insulator is used as the emitter and its current is I_E. The p-n junction is reverse biased and current through the junction is collector current I_C.

The devices with the double polysilicon layer of Fig. 8(b) show
in inverted bias conditions that essentially no electrons cross the insulat-
ing polysilicon from the conducting polysilicon to the semiconductor. This
is presumably due to the absence of the electrons in the conducting poly-
silicon.

C. NEGATIVE RESISTANCE COLLECTOR CHARACTERISTICS UNDER "INVERTED BIASING"

1. Negative Resistance Collector Characteristics for Inverted CID

The decreasing value of I_C/I_E at high emitter currents is not a
property of the insulator structure used, but rather a property of the device
geometry. For inverted biasing the device is a poor transistor structure
because of a large spreading resistance between the emitter (metal-insulator)
and base contact. This resistance can be modulated by the collector deple-
tion zone. A detailed discussion of this point is presented not only to
ensure that the correct interpretation is placed upon the I_C/I_E curves and
hence upon the insulator properties, but also because utilization of this
phenomenon may have significant device potential in its own right.

The data which were presented in Fig. 29 make use of only the
values of I_C when the collector voltage is zero. The common-base character-
istics of an inverted biased CID are presented in Fig. 30, with each curve
representing an increase of 5 mA in emitter current. It is apparent that
the increase in collector current becomes smaller for the same increment in
emitter current as the emitter current level is increased. The I_C vs V_C
curve for I_E = 60 mA would be almost superimposed upon the I_E = 30 mA curve.
The differential negative resistance characteristics which occur at either
high emitter currents or high collector voltages suggest that the collector
voltage modulates the emitter current and therefore the collector current.

2. Negative Resistance Collector Characteristics of Analogous Bipolar
Structures

The arguments advanced above make no reference to any particular
property of the metal-insulator emitter. It may therefore be suspected that
a bipolar device, without a metal-insulator emitter, would evidence the same

-57-
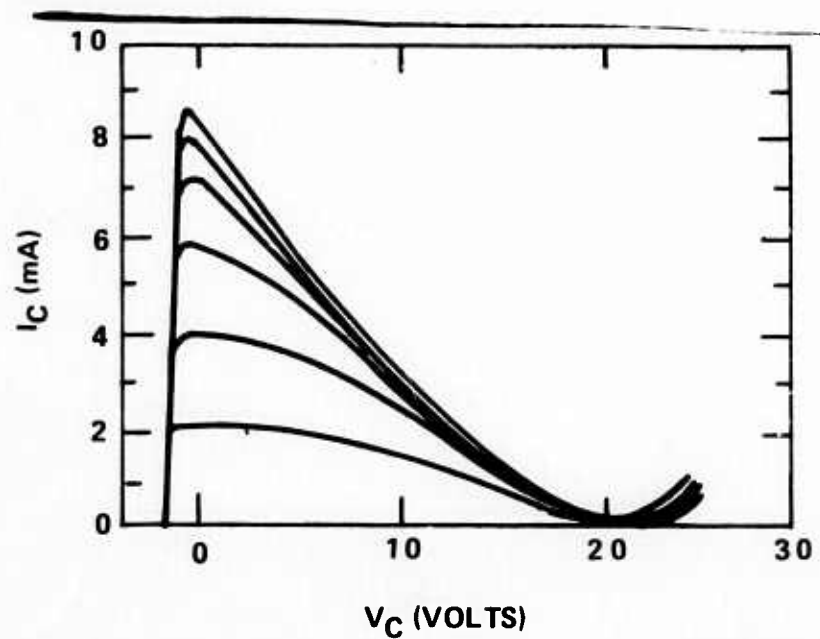
FIG. 30 Common-base characteristics of inverted biased CID. Curves correspond
to emitter currents equal to 5, 10, 15, 20, 25 and 30 mA. Note crowd-
ing of characteristics near V_C = 0.

behavior if its geometric construction is the same. This is found to be true. Figure 31 shows, in cross section, a CID structure and two analogous bipolar structures which were fabricated for comparison with the CID. The lateral dimensions of all three structures were produced using the same photoresist masks and therefore are essentially identical. The epitaxial layer's doping and thickness were also the same as the CID's.

It is to be noted that both bipolar structures differ significantly from ordinary transistor structures. The emitters of the bipolar structures are the diffused, limited-area, n^+ regions on the top of the structures. A well designed transistor structure would have the base contact connected directly to the p^+ region beneath the emitter of the middle structure. In contrast, both bipolar structures of Fig. 31 have a high-resistivity p region between the base contact and the emitter. Because the p region is lightly enough doped, the depletion region associated with the reverse-biased collector can completely sweep out this region, further increasing the base-to-emitter resistance. The grounded-base collector characteristics of the middle device of Fig. 31, which has a p^+ region surrounding the n^+ collector, are presented in Fig. 32. Note that there is a pinch-off of collector current to nearly zero at approximately 14 V, slightly below that observed in the analogous CID structure whose characteristics are shown in Fig. 30. The grounded-base characteristics of the bottom structure of Fig. 31 are shown in Fig. 33. There is a clearly defined region of negative differential resistance, but no reduction of the collector current to zero. This is not surprising because the n^+ emitter region for this device is not surrounded by a heavily doped p^+ region; thus "punch-through"[10] of the collector depletion region to the emitter is possible. Because the emitter junction is nearer to the collector than is the surface of the device, breakdown via the "punch-through" mechanism will occur at voltage below pinch-off of the base and emitter region. Therefore, the collector current is not reduced to zero as the collector voltage is increased.

These analogous bipolar structures show a reduced value of I_C/I_E at high emitter currents similar to that of the inverted biased CID. A

-59-
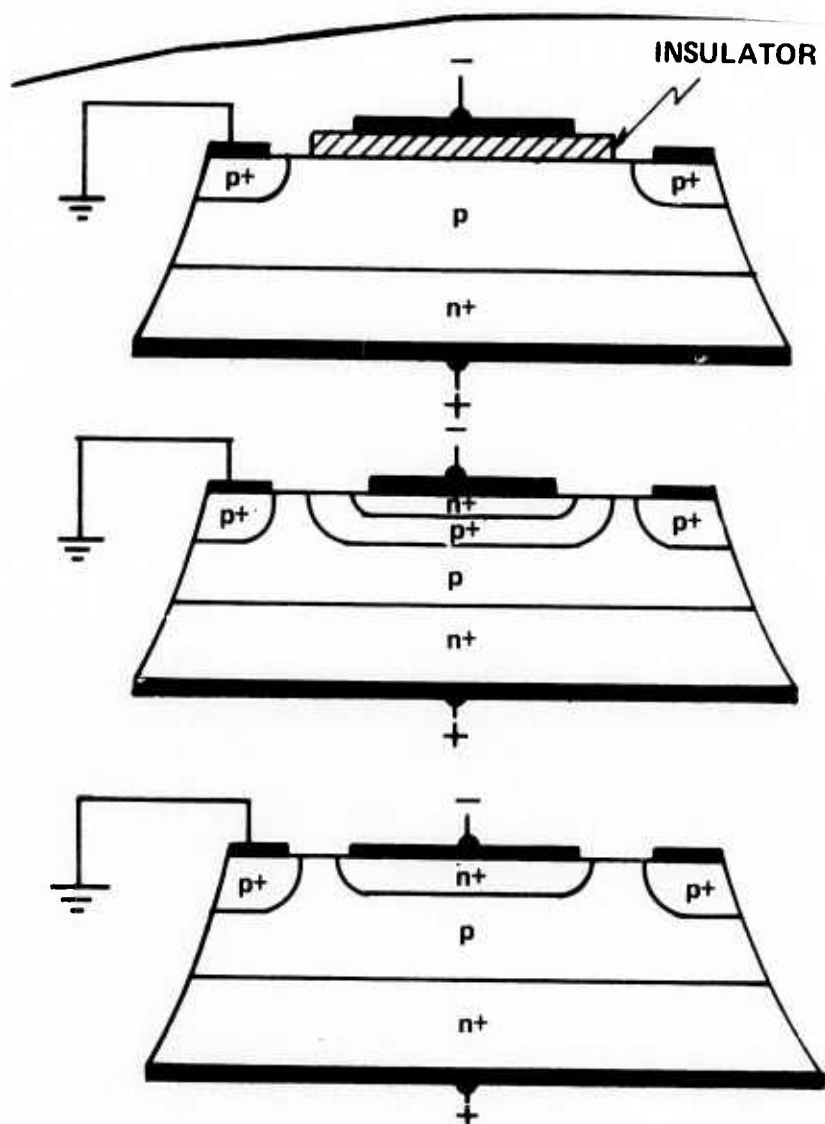
FIG. 31 Cross-sectional views of inverted biased CID structure (top) and two analogous bipolar structures. All three devices were fabricated using the same photoresist masks.
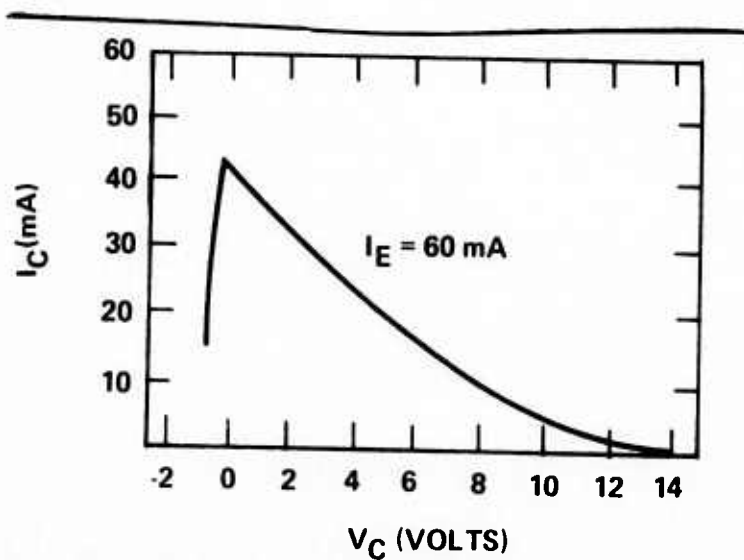
FIG. 32 Grounded-base characteristics of device shown in middle of Fig. 31.
Only single trace is shown (for I_E = 60 mA) because instabilities due
to negative resistance occurred when curve tracer was set to automatic
step emitter current.
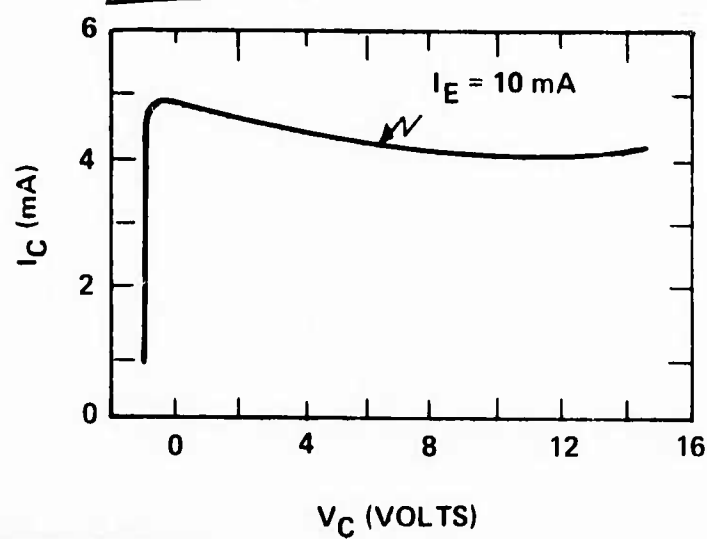
FIG. 33 Grounded-base characteristics of device shown at bottom of Fig. 31. Only single trace is shown (for I_E = 10 mA) because instabilities due to negative resistance occurred when curve tracer was set to automatic step emitter current.

comparison of the I_C/I_E vs I_E curves for the middle structure of Fig. 31 is presented in Fig. 34. The similarity in the shape of these curves proves that the drop-off in I_C/I_E at high I_E of the CID is not a property of the insulator of the CID itself. The increasing values of I_C/I_E with increasing I_E at low values of I_E are clearly a property of the metal-insulator emitter, however. The bipolar structure from which the date of Fig. 34 were obtained was purposefully fabricated with a relatively low concentration of donors in its emitter region (barely enought to compensate for the p^+ diffusion which underlies it) so that, like inverted biased CID's, its emitter efficiency would not be high. This accounts for the fact that I_C/I_E is not approximately equal to unity for low emitter currents.

It will be demonstrated in the sequel that the drop-off in I_C/I_E at high I_E is caused, even at zero collector bias, by the voltage drop between base contact and emitter region for both the bipolar and CID structure. This current-induced voltage drop contributes to the total voltage drop between collector and emitter, thus causing a widening of the collector depletion zone even though the collector-base voltage drop is small. An analogous situation occurs in field-effect transistors in the phenomenon of current saturation in which the source-drain current is limited by a pinch-off of the gate's depletion zone even though the source-gate voltage is zero.[11] This excess voltage, which is required to be applied between the emitter and base contacts, also accounts for the fact that in a common emitter mode both the inverted biased CID and the analogous structure of Fig. 31 require an unusually large collector voltage compared to conventional bipolar transistors for the collector current to peak, as illustrated in Fig. 35.

3. Explanation of Negative Differential Resistance in "Inverted Biased" CID and Analogous Bipolar Structures

An analysis of the negative differential resistance can be given in great detail in terms of doping densities and dimensions of the device. Such an effort is not worthwhile because the structures which have been used are far from an optimum structure for exhibiting the phenomenon. However, it is possible to engage a more general argument which has some additional benefit in that it is simple.

-63-
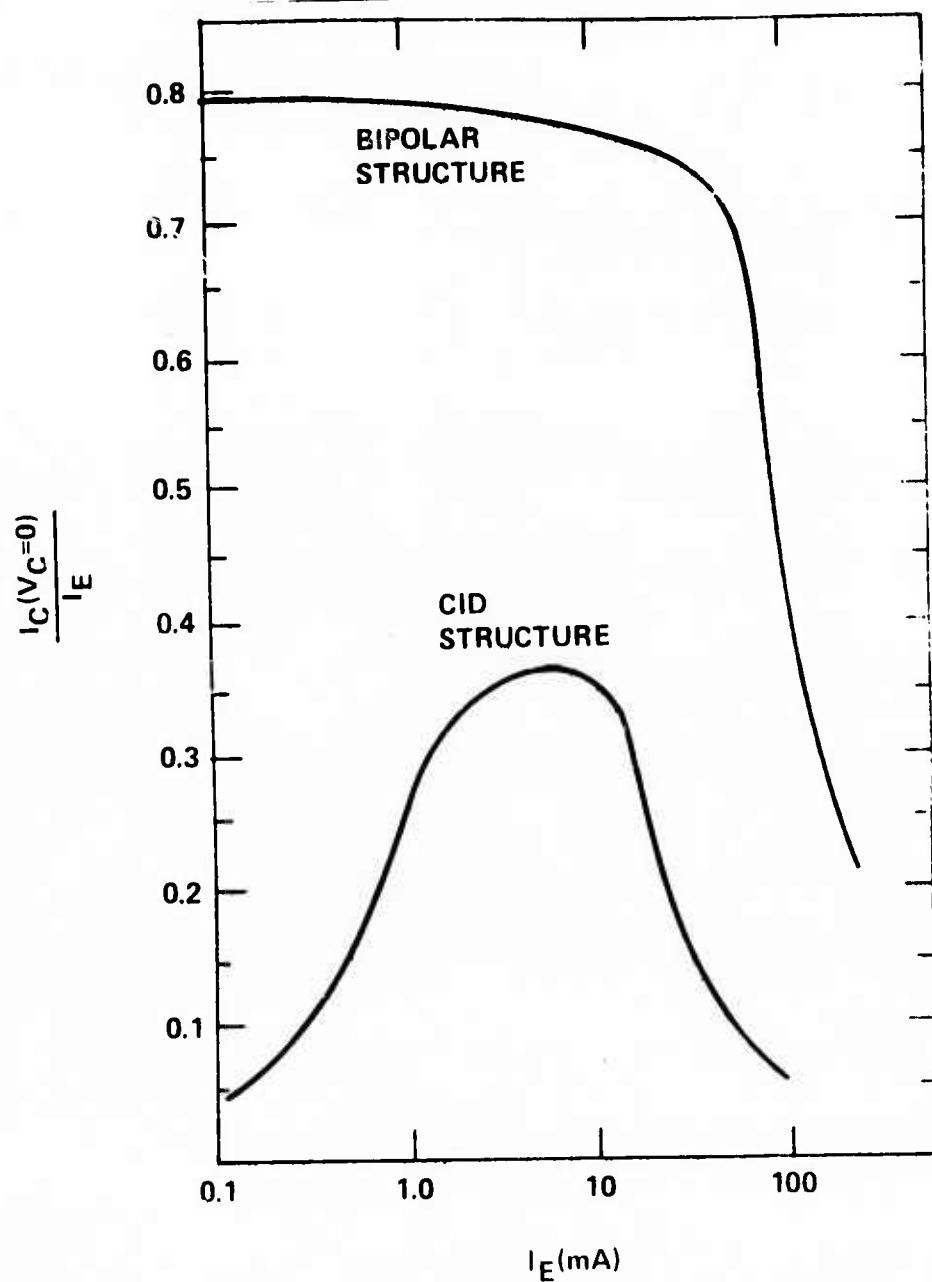
FIG. 34 Comparison of I_C/I_E vs I_E for inverted biased CID and analogous bipolar structures. Structure studied is shown in cross section in two upper illustrations of Fig. 31.
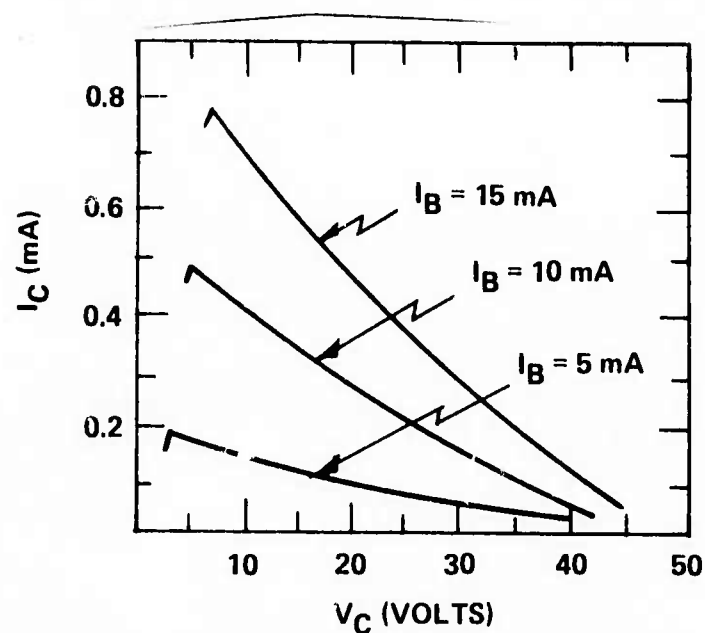
FIG. 35 Common-emitter characteristics of an inverted biased CID whose epitaxial layer (and hence pinch-off voltage) was larger than the device whose common base characteristics are shown in Fig. 30. Note that collector current stops increasing at unusually high voltages (2-7 V) compared to a well designed bipolar transistor. This high voltage for peak collector current is caused by large emitter-base resistance.

The basis of the description is that the device can be represented as a combination of a bipolar transistor and a junction field-effect transistor. A composite model of this device is presented in Fig. 36. For clarity we redefine the terminal connections of the middle device of Fig. 31. The "emitter" region remains the n^+ region and is surrounded by the p^+ region. The "base" region is the p^+ region which surrounds the emitter. Note that there is no _external_ connection to this base region. The "base" region will also be termed the "drain" interchangeably. The "source" of this device is the annular p^+ diffused region which in Fig. 31 is grounded. The "collector" region is identical to the "gate" contact in our new nomenclature. Note that considered as a group, the "source," "drain" ("base") and "gate" ("collector") form the usual terminals of a junction field-effect transistor. Note also that the "emitter," "base" ("drain") and "collector" ("gate") together form the usual terminals of an n-p-n bipolar transistor.

Let R be the low-field resistance between source and drain as measured when the source-to-gate voltage is zero. If V_p is the "punchthrough" voltage of the gate's (collector's) depletion region to the top surface of the device, one would expect that the maximum source current I_m with $V_C = 0$.

$$I_m \approx 1/3 \; \frac{V_p}{R} \tag{2}$$

as in analogy with JFET structures.

The collector current will be made equal to the emitter current which in turn, following conventional bipolar theory, should be β times larger than the source current. Here β is the conventional common emitter current gain of the bipolar transistor. Since the collector current will be zero when $V_C = V_p$, we expect that the minimum absolute value of the negative differential resistance R_N will be given by

-66-

FIG. 36   Composite model of equivalent circuit of inverted biased CID and analogous bipolar structure.
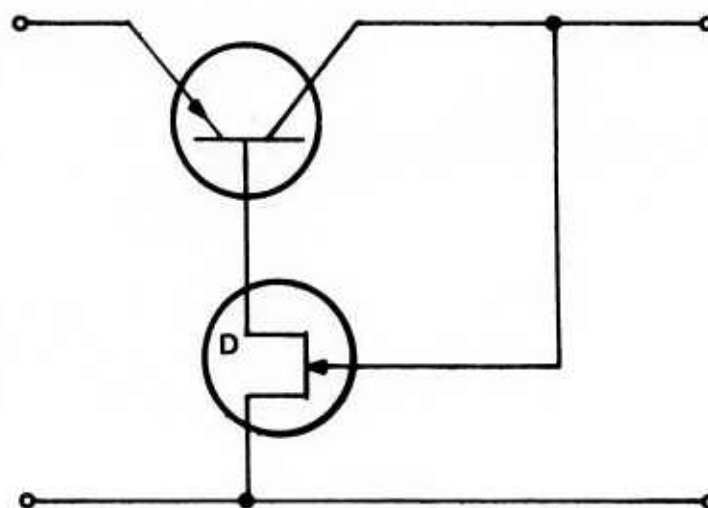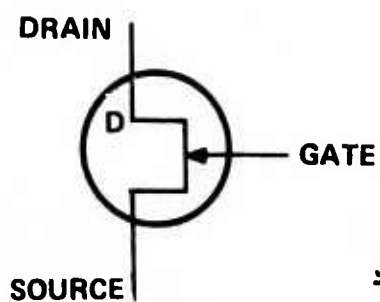
$$(R_N) \approx \frac{V_P}{\beta I_m} \approx \frac{3R}{\beta} \quad .$$

Thus, we conclude that the magnitude of the differential negative resistance should increase if the source-to-drain resistance increases and decrease if the emitter efficiency of the device increases. These relationships have been confirmed experimentally. More heavily doped emitter regions, which increase the emitter efficiency, lower the magnitude of the observed negative resistance. Similarly, increasing the source-to-drain resistance by employing higher resistivity epitaxial layers has resulted in higher absolute values of the negative differential resistance. The common-emitter characteristics shown in Fig. 35 were in fact recorded from such a device. The higher value of the negative differential resistance compared to the devices whose characteristics are illustrated in Fig. 32 is also accompanied by a smaller value of I_m, as would be expected from our analysis.

The theory outlined above predicts that the source-to-emitter current, as well as the collector current, will be modulated by variations in the collector voltage. This is confirmed in experiments. Figure 37 presents the I-V characteristics of the emitter-source terminals for various values of the collector voltage. The I-V relationship at even zero collector bias does not appear as that of an ideal p-n junction because of the internal resistance built into this structure. Higher values of collector voltage increase the source-emitter resistance as expected.

A complete analysis of the high-frequency behavior of the device would have to include transit-time effects. Such an analysis would differ greatly for small changes in device dimensions, and is not appropriate for the unoptimized structures experimentally examined. However, it should be pointed out that the criterion for the high-frequency limit of a JFET takes another form for these negative differential resistance devices. A simple estimate of the upper limit of amplification of a JFET is obtained from the ratio of the maximum transconductance to the minimum gate capacitance.[11]

I_B (1 mA/div.)

V_B (2 V/div.)
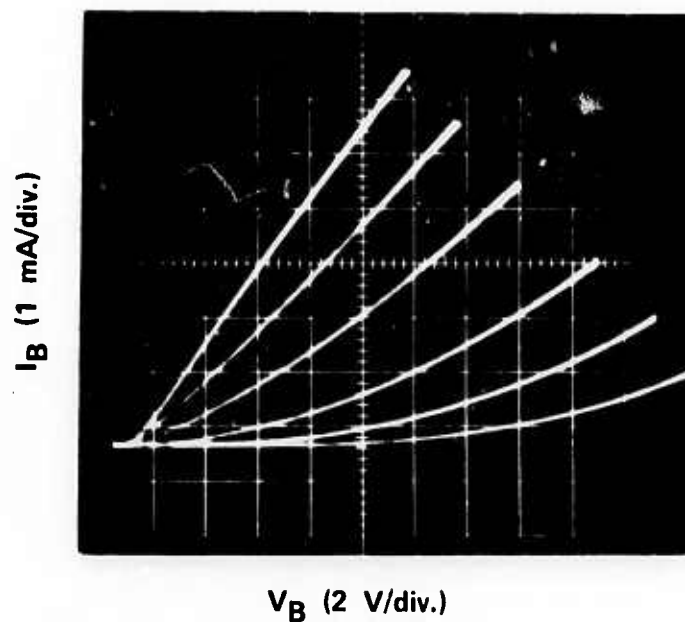
FIG. 37 Current-voltage characteristics of emitter-source terminals of middle device of Fig. 31 for various values of collector bias. (V_C = 0, 2.5, 5.5, 9.5, 14.0 and 16.5 V.) Highest conductance corresponds to V_C = 0 and lowest conductance corresponds to V_C = 16.5 V.

The negative conductance of the negative differential resistance is greater by the factor β than the transconductance of the JFET. Higher frequency of operation is therefore expected for the negative differential resistance device if comparable capacitance can be obtained. A device whose capacitance was 6 pF and whose dc differential resistance was $\approx$ - 2000 Ω, was examined on an UHF netowrk analyzer. Negative resistance was observed to approximately 10 MHz, which is approximately $1/2\pi C |R|$.

4. <u>Negative Resistance Characteristics of Analogous Bipolar Structures at UHF Frequencies Under Inverted Bias</u>

The impedance of the middle device of Fig. 31 was measured under inverted biasing between 0.5 and 500 MHz.[12] As was stated earlier, the low-frequency negative resistance disappeared for frequencies above 20-40 MHz, in agreement with the simple considerations which were based upon a low-frequency model. All these present measurements were carried out on a GR network analyzer.

An anomally was noted, however, for certain bias conditions. At these special bias conditions, a negative resistance was observed for much higher frequencies (300-400 MHz). The bias conditions for which the UHF negative resistance was observed can be described precisely by examining the dc I-V characteristics of the device under inverted biasing which are presented in detail in Fig. 38. The special bias points are noted as (I_1,V_1), (I_2,V_2) and $I_3,V_3)$ in this diagram and any other similar points where the collector I-V characteristics change from a positive to a negative resistance. Different emitter currents are, of course, the parameterized quantities in the family of curves of Fig. 38, with the largest emitter current corresponding to I_3 and the smallest to I_1.

Near-critical bias points, where the dc collector characteristics change sign, a negative resistance is observed at UHF frequencies. The negative resistance is observed between 300 and 500 MHz at such dc bias points with the frequency band of negative resistance not being particularly sensitive to which bias point is chosen. A typical plot of resistance as a function of frequency for one particular bias point is shown in Fig. 39.

-70-
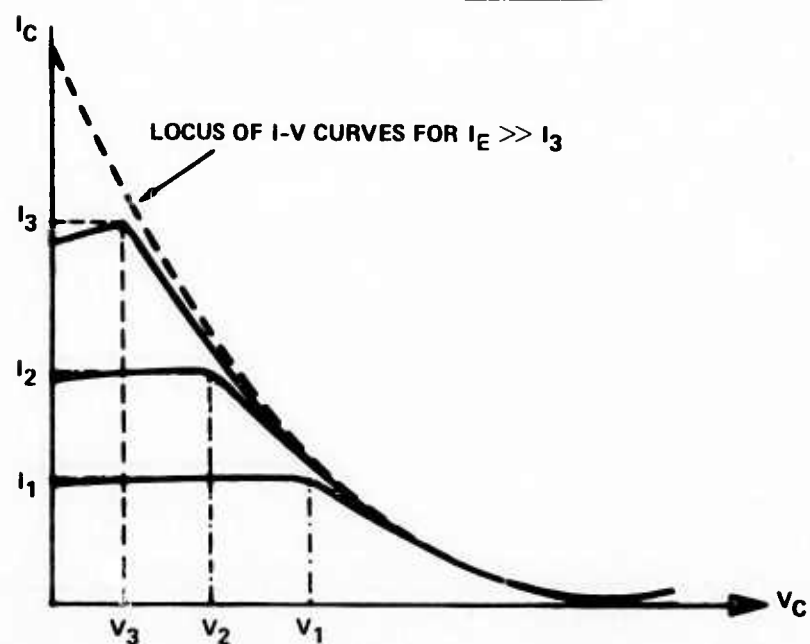
FIG. 38 Detailed representation of grounded-base I-V characteristics of middle device of Fig. 31. The points (I_1, V_1), (I_2, V_2) and (I_3, V_3) represent the bias conditions at which $dI/dV = 0$. Applied emitter currents increase as $I_1 \rightarrow I_2 \rightarrow I_3$.
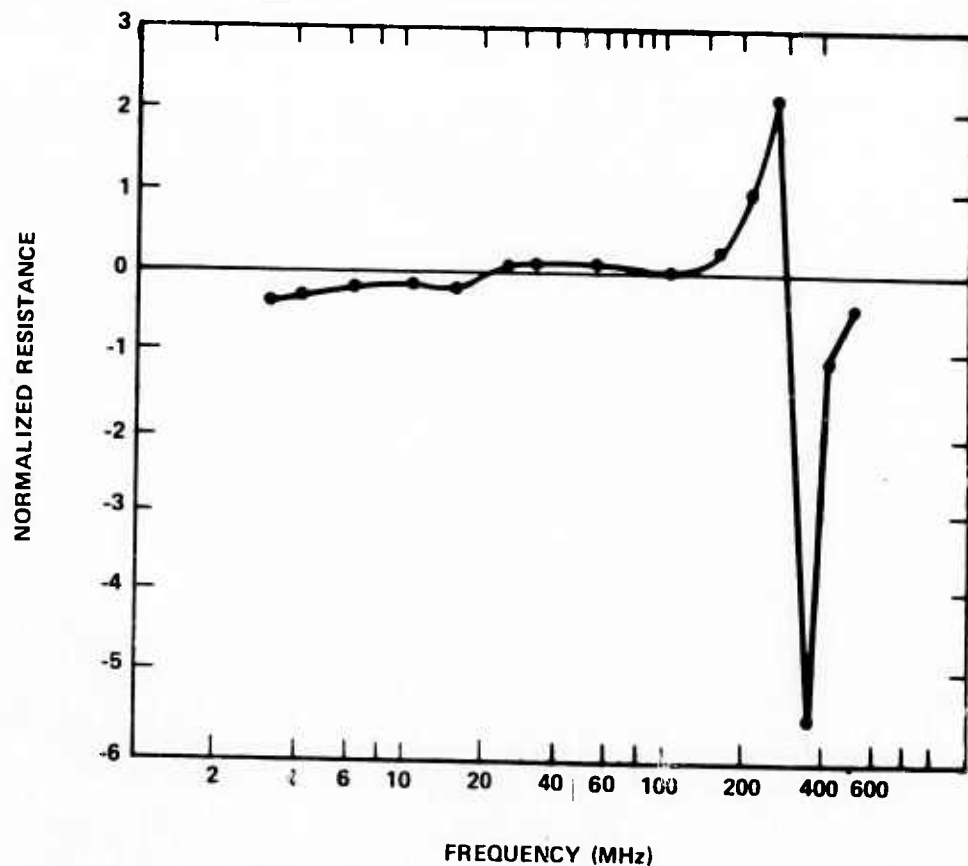
FIG. 39 Measured resistance of the middle device of Fig. 31 as a function of frequency when dc characteristics (I_E and V_{CB}) were chosen so that $dI_C/dV_C = 0$.

The origin of this negative resistance is certainly due to transit-time effects. Two significant transit times will appear in the device structure of the middle diagram of Fig. 31. These are the transit-time of diffusion of base minority carriers from the emitter to the depletion region of the collector and the drift time of base majority carriers from the "source" to the "drain" (base). The drift transit time of carriers across the collector depletion zone is negligible compared to these other transit times.

The drift transit time of base majority carriers from "source" to "drain" of the device cannot be less than

$$\tau_1 = d_1/v_S$$

where v_S is the scattering-limited velocity and d_1 is the "source" to "drain" distance. For these devices $d \approx 2.5 \times 10^{-3}$ cm, and therefore

$$\tau_1 > 2.5 \times 10^{-10} \text{ s} \quad.$$

The diffusion transit time of carriers across the neutral region between the emitter and collector junctions can be estimated as follows. We estimate the width of this neutral region as 2 μm the diffusion transit time τ_2 across this neutral region will be given by

$$\tau_2 = w^2/2D$$

where we take take D equal to the diffusion constant for holes (≈ 10 cm^2/s). Therefore, $\tau_2 = (2 \times 10^{-4})^2/20 = 2 \times 10^{-9}$ s.

The sum of τ_1 and $\tau_2 \approx \tau_2 = 2 \times 10^{-9}$ s. The frequency of negative resistance f_N will be given by

$$f_N \approx \frac{4}{3} \text{ (transit time)}^{-1}$$

This predicts a negative resistance at a frequency of 600 MHz, in satisfactory agreement with the observation of 300-500 MHz.

SECTION 8

FET STRUCTURES USING CID "INSULATORS"

One could reasonably inquire as to whether any of the CID insulator structures could be used as the insulator beneath the gate of an IGFET structure. There are two possible motives for this. First, one could conceive of a variation in the insulator structure which provides a thicker or intrinsically less conductive layer so that an IGFET structure could be produced.[13] One possible advantage of such a structure would be, perhaps, greater radiation resistance if no silicon dioxide were present in the structure. The other purpose of such a structure would simply be to provide an alternative method of studying the extent of inversion of a CID structure by measuring the conduction between source and drain electrodes rather than by capacitance measurements or by inferences from the conduction through the insulator.

Such structures have not yet been extensively studied, partially because of technological difficulties in their fabrication which have only recently been solved. The only structure of this type which has been fabricated is shown in cross section in Fig. 40. The polysilicon insulator layer was chosen to be 0.3-0.4 μm thick rather than the 0.2 μm used in the CID structures described in Sec. 3 in an effort to make the layer slightly less conductive. The polysilicon layers were somewhat awkward to use in these structures because they were not easily and precisely etched.

Etching was necessary in order to make contact to the previously diffused source and drain regions of this enhancement-mode p-channel device. Etching of the polysilicon by water HNO_3-HF etches tended to leave a rough residue through which ohmic contact could not be made without significant etching into the single-crystal layer. This prolonged etching tended to undercut the gate contact significantly. A clean removal of the polysilicon was possible by using a water-CrO_3-HF etch. This etch, although it did not significantly attack the single-crystal silicon, did undercut the gate contacts very severely. Use of metallization other than chromium-gold might

-75-
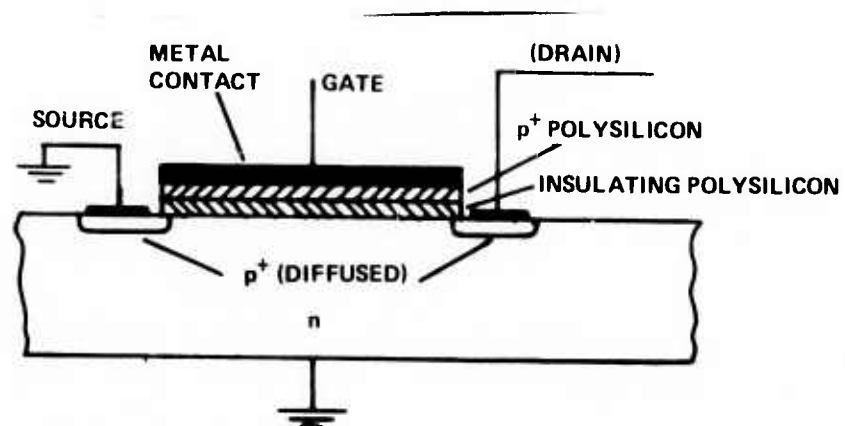
FIG. 40 Cross-sectional diagram of p-channel IGFET-type device with polysilicon used as the insulator.

have alleviate this problem. Attempts should be made t: use amorphous silicon layers in further studies of structures of this type. These layers may be more easily etched and can be considerably thinner than polysilicon and still provide the same insulating properties.

The structure of Fig. 40 did yield some interesting results, however. The source-drain current as a function of source-drain voltage of the structure of Fig. 40 is presented in Fig. 41, with the gate voltage appearing as a parameter. The interesting results of this experiment depend critically on the understanding that the polarity of gate voltage shown in Fig. 41 is opposite to what one would expect for a p-channel device. The steps in gate voltage were positive with respect to the substrate, therefore indicating that holes were being injected from the polysilicon. Applying a negative voltage to the gate, which would normally attract holes to the gate region, is not as effective in increasing the drain current as the positive bias shown in Fig. 41. The application of a negative bias causes a greater conduction of holes through the "insulator" to the gate than to the drain of the device.

I_D (5 mA/div)

V_C (1 V/div) ⟶
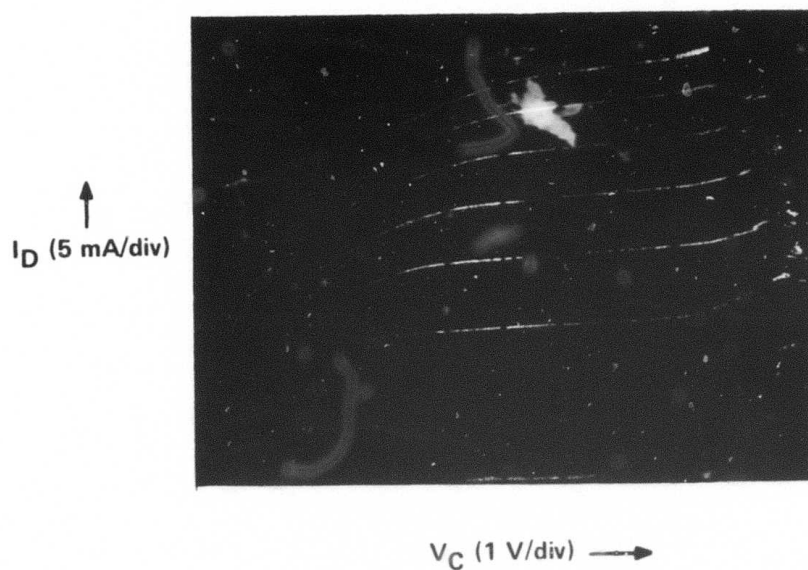
FIG. 41 Drain current as a function of drain voltage for the device structures of Fig. 40. Gate voltage is stepped in *positive* sense with respect to substrate. Gate voltage step is 0.2 V with lowest gate voltage equal to 0 V (at smallest drain current) and highest gate voltage equal to +1.6 V (at highest drain current).

SECTION 9

THEORETICAL CONSIDERATIONS OF DC IMPEDANCE STATES
OF CONTROLLED INVERSION DEVICES

The previously described I-V and C-V data of the CID enable some quantitative conclusions to be drawn regarding the minority carrier distributions present in each state and the theoretical requirements for the appearance of the CID phenomenon. It is the purpose of this section of the report to state such conclusions with as much generality as possible.

A. HIGH-IMPEDANCE STATE

In the high-impedance state a much larger voltage appears across the CID's semiconductor surface depletion zone than would be present if a similar structure, but one with a "perfect" insulator, were chosen for fabrication. The simplest consideration which leads to this result is the deduction which follows from an assumption that, in fact, an inversion layer does form biases which would cause inversion for a device which had a perfect insulator. In such a case the maximum width W_m of the surface depletion zone is given by

$$W_m \approx \sqrt{\frac{4\varepsilon_s kT}{q^2 N} \ln(N/n_i)}$$

where N is the (assumed uniform) donor or acceptor density of the semiconductor region adjacent to the insulator and n_i is the intrinsic carrier concentration of the semiconductor.[14] This applied voltage, when the maximum depletion layer width is reached, is approximately $2\varphi_B$, where φ_B is the potential difference between the Fermi level and the intrinsic level of the semiconductor at equilibrium.[14] W_m is typically less than 1 μm for the devices studied, and the voltage at which W_m is attained is less than 1 V.

If the assumption is made that only this voltage appears across the semiconductor, then the remainder must appear across the insulator.

Less than 0.5 V can appear across the junction, since in the high-impedance state hardly any current is drawn.) The electric field across the insulator under such an extreme assumption could be as high as 3.5×10^7 V/cm (70 V across a 200 Å insulator), an obvious impossibility since the dielectric breakdown strengths of all insulators used were less than 10^7 V/cm. The only alternative is for the high-impedance state to exist without sufficient inversion to prevent the continued widening of the surface depletion zone to much larger widths than that given by W_m.

This is illustrated in Fig. 42, which compares the surface depletion zones of three devices: an ideal MIS structure (with a perfect insulator), the CID device, and an ideal Schottky contact. At low biases all devices have substantially the same depletion widths (neglecting small variations because of work function differences, etc), but even more importantly, all three devices have depletion widths which increase monotonically with applied reverse bias to the surface. At intermediate biases $(V > 2\varphi_B)$, the depletion width of the ideal MIS is pinned at W_m, as shown in the middle electric field diagram of Fig. 42, whereas W_{CID} and $W_{Schottky}$ are both still nearly equal and increasing with bias. This corresponds to the high-impedance state of the CID with relatively high biases applied to the device. The wide depletion width of the CID is directly confirmed by many measurements, including the C-V data of Figs. 10, 15, 17 and 18.

Still higher baises applied to the devices and a series resistor result in a transition to the low-impedance state of the CID and a collapse of the CID's depletion zone down to a wioth approximately equal to that of the ideal MIS structure. This point will be discussed in Sec. 9B in more detail. The depletion zone width of the Schottky barrier will still increase, however, as long as breakdown does not occur.

It is apparent that in the high-impedance state of the CID $pn < n_i^2$. If $pn = n_i^2$, then one would obtain exactly the results of the ideal MIS with only narrow depletion widths possible. (Strictly speaking, it would be possible to have $pn \gtrsim n_i^2$ for the high-impedance state if the minority carrier concentration, say p, were much less than the equilibrium
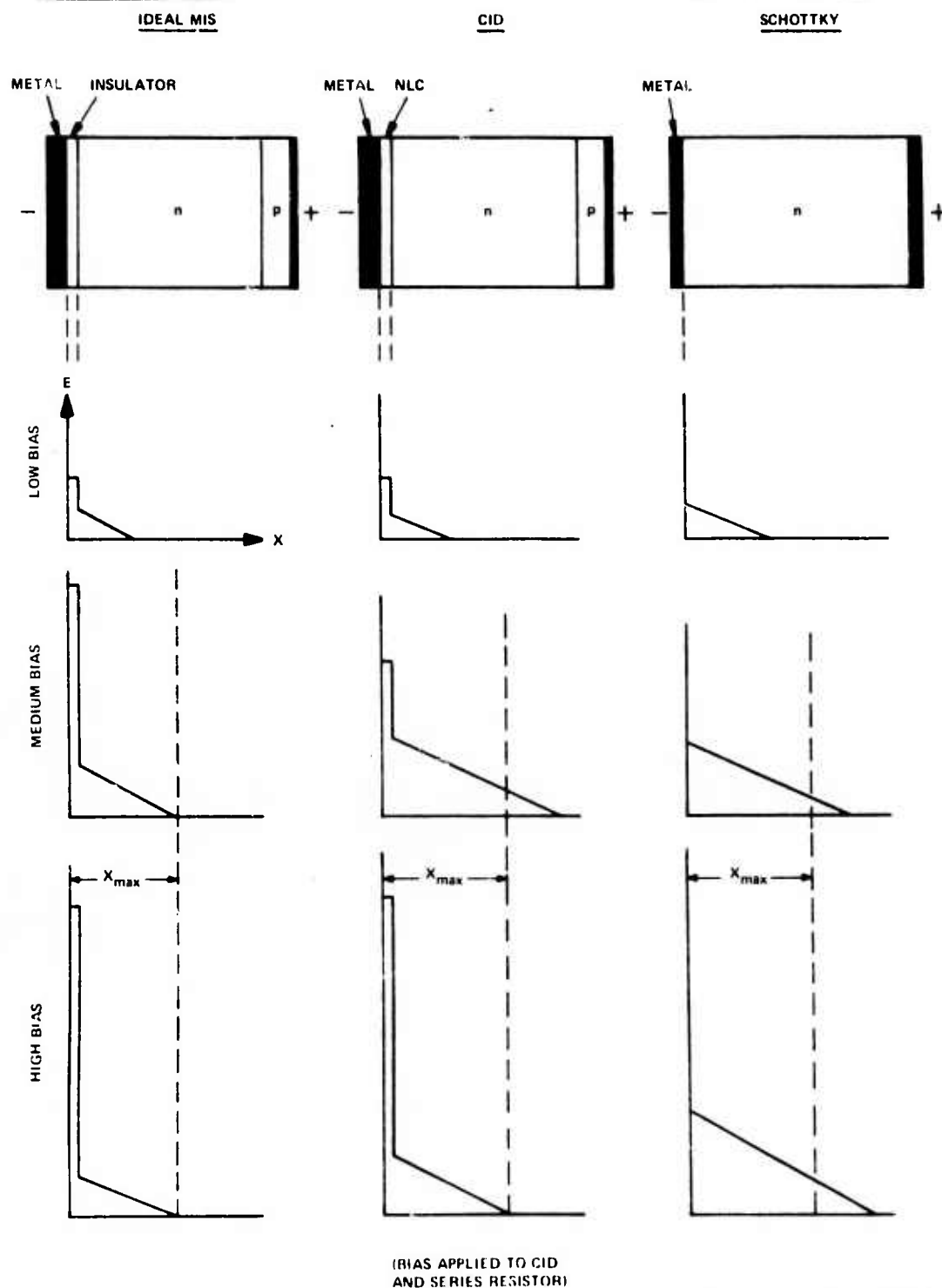
FIG. 42 Comparison of depletion zones of three structures, ideal MIS, CID and Schottley barrier device, as a function of bias. Approximate electric fields in depletion approximation are plotted vs distance.

value p_{eq}, but with $n \gg n_{eq}$; this is viewed as unlikely since this condition is more likely to result in the intermediate level conductivity state, as will be discussed in the sequel.) In order to keep the minority carrier concentration low, the insulator must be able to dissipate all of those minority carriers injected into or generated within the surface semiconductor region. This dissipation could be either by direct conduction or by annihilation by majority carriers entering the semiconductor from the opposite direction. The latter process may not be important in many situations, however, since if $pn < n_i^2$, one would expect generation to exceed recombination both for surface or volume processes if Hall-Schockly-Read recombination processes are dominant.[15]

How conductive the insulator must be to prevent the build up of minority carrier density may be estimated as follows. The surface generation of electron-hole pairs is neglected for the mement. (We are first interested in estimating the lower limit of necessary conductivity of the insulator; one method of doing this is to assume zero surface generation.) The generation current I_{gen} in the depletion zone of the device will be given by

$$I_{gen} = 1/2 \; q \; \frac{n_i}{\tau_o} \; WA$$

where τ_o is the effective lifetime within the depletion zone of width W and A is the area of the device. Now

$$W = \left(\frac{2 \epsilon_s V_s}{qN} \right)^{\frac{1}{2}}$$

where V_s is the voltage drop across the depletion zone of the semiconductor. If no inversion layer has formed at all (we realize that is is somewhat of

an idealization, since the data of Sec. 5 indicate that the development of
the inversion layer in some devices can be gradual with increasing collector
voltage), then

$$\epsilon_{in} E_{in} = \epsilon_s E_{si}$$

where ϵ_{in} and ϵ_s are the dielectric constants of the insulator and semicon-
ductor, respectively, and E_{si} is the electric field at the semiconductor
surface.

The total minority carrier current across the insulator will be
the sum of I_{gen} and any injected current from the junction. The injected
current I_j will be given by

$$I_j = \alpha_o (I_{gen} + I_{maj})$$

where I_{maj} is the majority carrier current injected from the insulator into
the semiconductor and α_o is the common-emitter current gain of the emitter
junction. considered as a part of a conventional three-terminal bipolar
junction transistor. The factor α_o will be a strong function of bias and
will generally be smaller for many of our devices than for common transistors,
since the usual geometry of a CID is not that of efficient, high current-
gain transistors.

Finally, combining the above results we find that minority carrier
current across the insulator I_{min} must exceed

$$I_{min} \geq I_{gen} + \alpha_o (I_{gen} + I_{maj}) \text{ or}$$

$$I_{min} \geq (1 + \alpha_o) \frac{qn_i}{2\tau_o} \left(\frac{2\varepsilon V_s}{qN} \right) A + \alpha_o I_{maj}$$

if no inversion has formed. By using the relation $V_s = 1/2 \, E_{si} W$ and the relation between E_{si} and E_{in} this may be cast in a form which gives a requirement for the "minority carrier conductivity" of the insulator. Such a relationship is complex because it depends upon the relative conductivities of electrons and holes through the insulator. The ratio of electrons to hole current may be expected to change with varying voltage across the insulator, as was explicitly shown in Sec. 7B. For the case of "inverted" bias, and to the extent the current of minority carriers is limited by availability of their supply at the semiconductor-insulator interface.

The limits to the high impedance state may be discussed in principal by combining all the variations of the ratio of I_{maj}/I_{min} across the insulator into a single factor f when we write $I_{maj} = fI$. In Fig. 43 we choose as a point of reference a position just within the semiconductor given by X_1. For this particular device we have

$$I(X_1) = fI \quad .$$

The electronic current I_n will be given by

$$I_n(X_1) = I_{gen} + I_{sur} + \alpha_o I$$

where I_{sur} is the surface generation current, I_{gen} is the bulk generation current and we assume negligible recombination. Combining these two equations, we have, since $I = I_n + I_p$,
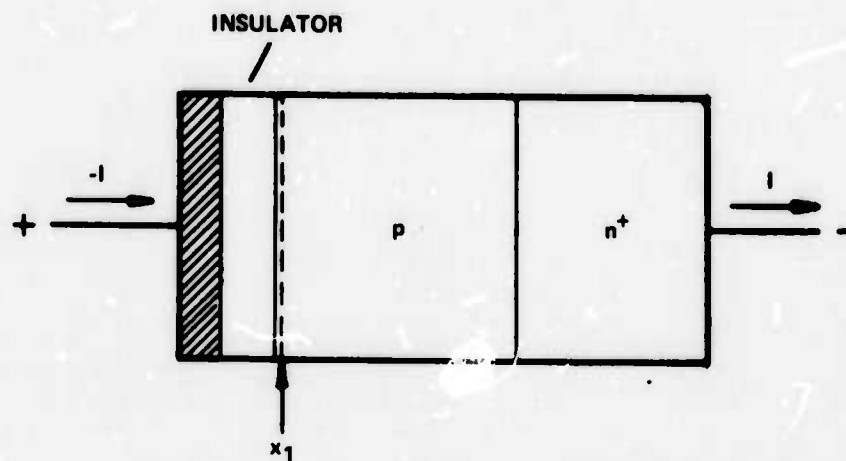
FIG. 43 Cross-sectional view of metal/insulator/p/n$^+$ diode. The position x, is just within the semiconductor surface.

$$I = \frac{I_{gen} + I_{sur}}{1-(f + \alpha_o)} \quad .$$

It is clear that if $f + \alpha_o = 1$, the assumptions of the model (that $pn < n_i^2$) will be violated and that the bias conditions under which $f + \alpha_o = 1$ mark the limit of the high-impedance state. More exactly, if the sum of the small signal quantities $\partial f/\partial V$ and $\partial \alpha_o/\partial V$ is equal to unity at a voltage bias V, the $V = V_{th}$ for a CID diode.

Different CID structures (with regard to insulator material and method of deposition, semiconductor doping and geometry) can have quite different variations of f and α_o with voltage bias. It is likely that the appearance of a "virgin state" described previously may be related to a change of the factor f as a result of permanent trap filling within the insulator material of those structures which exhibit the phenomenon.

The requirement that $f + \alpha_o = 1$ for the attainment of the threshold voltage has been quantitatively demonstrated for some devices in some special situations. In Sec. 7A, common-base I-V characteristics were demonstrated for three-terminal devices. If small emitter currents are used, then the switch-back to lower voltage states when higher currents are observed does not occur. The limitation of minority-carrier current to the base is apparently the reason for this, since it is this current which is limited in the common-base configuration. (Higher values of I_E do permit a switch-back, but not as robustly as in the common-emitter configuration.)

As stated in Sec. 7A, near the voltage where V_{th} would be observed in the common-emitter configuration, the common-base current gain exceeds unity. (The voltage at which is occurs is slightly greater than V_{th} for the same reason that breakdown voltages of bipolar transitions are always higher in grounded-base than in grounded emitter configurations.) The increase in common-base current gain above unity is essentially a restatement that $f + \alpha_o > 1$.

B. LOW-IMPEDANCE STATE

It is interesting to note how easily the pn product may be driven above its equilibrium value in the reversed-bias surface depletion layer of a CID where, in general, we expect carriers of both signs to contribute to substantially to the conduction. This is in contrast to the more usual case of the collector region of a bipolar transistor where carriers of only one sign substantially contribute. But even in this case the pn product may exceed n_i^2. The expectation that carriers of both signs will substantially contribute is indicated, but not proven, by the "inverted bias" experiments of Sec. 7B.

The smallest concentration of carriers within the surface depletion zone which can support a current density J will be obtained if saturated drift velocity is present everywhere throughout the depletion zone. Clearly, this will not be possible everywhere throughout the depletion zone, and therefore even larger carrier densities will be required than those obtained by this estimate.

Let us suppose that $J_n = J_p$, then if saturated velocity is obtained,

$$J/2 = J_n = qv_s n$$

and

$$J/2 = J_p = qv_s p$$

where v_s is the saturated velocity for both electrons and holes. Then

$$np = \left(\frac{J}{2qv_s}\right)^2$$

and np will exceed the room temperature n_i^2 if

$$J \geq 2qv_s n_i = 2(1.6 \times 10^{-14})10^7 (1.5 \times 10^{10}) \text{ A/cm}^2$$

or

$$J > 5 \times 10^{-2} \text{ A/cm}^2$$

where we have taken $v_s = 10^7$ cm/s for silicon. This current density is less than that observed for the minimum sustaining current of the low-impedance state of all CID's which have been fabricated and is within the range of current densities actually observed in the high-impedance state of a few device types.

The pn product may therefore easily exceed n_i^2 even though the surface depletion layer is reverse biased. If $J_n \neq J_p$, then, of course, a somewhat larger current density would be required for $pn \geq n_i^2$.

If not only $pn > n_i^2$, but the minority carrier density (in Fig. 43) in the region of the semiconductor exceeds its equilibrium value n_{eq}, then it is clear that the surface will invert with a sustaining surface voltage equal to that for inversion of an ideal MIS structure if $n = n_{eq}$ or at even a lower voltage if $n > n_{eq}$. If $n \approx n_{eq}$, then the voltage drop across the semiconductor surface will be $\varphi_B = ekT/q \ln(N/n_i)$ and the total voltage drop across the diode will be given by

$$V(I) = V_{in} + 2kT/q \ln (N/n_i) + V_J(I)$$

where V_{in} and $V_J(I)$ are the voltage drops across the insulator and junction, respectively.

V_{in} is typically $5 \times 10^{-2} - 6 \times 10^{-1}$ V, depending upon the insulator. The voltage drop across the semiconductor surface, $2kT/q \ln N/n_i$, is typically 0.1-0.5 V depending upon doping and 0.7 V $< V_J(I) < 1.0$ V for current densities of interest. The total voltage which one calculates is therefore

between 1 and 2 V, which agrees with the 1.2-2.2 V sustaining voltage observed for the low-impedance state of most CID's.

C. INTERMEDIATE CONDUCTIVITY STATE

The third, intermediate conductivity state of the CID is not observed in all structures. In particular, it is not observed for poly-silicon and amorphous-silicon insulator layers. As noted in Secs. 3 and 4, devices made with these materials are distinguished qualitatively from devices fabricated from silicon oxides and nitrides by having the current carried across them primarily by carriers which are the minority carriers of the semiconductor surface region. The ratio of I_{maj}/I_{min} for the silicon insulators does not appear to change as rapidly with bias as does the ratio for other insulator materials.

This observation can be connected in at least a qualitative way with the preceding discussion. An argument similar to that advanced in Sec. 9B, will also demonstrate that it is almost certain that $pn > n_i^2$, for the surface depletion layer when the device is in the intermediate conductivity state. It is clear, however, that since the sustaining voltage of the inter-mediate state is typically 6-12 V, then the minority carrier density does not exceed the equilibrium minority carrier density, or else the sustaining voltage would below (approximately) $2kT/q \, \ell n \, N/n_i$. The only way $pn > n_i^2$ with, say, $n \sim n_{eq}$ is for $p > p_{eq}$. This would come about if the current in the intermediate state were carried predominately by majority carriers (holes for the case of Fig. 43) of the surface semiconductor region. This deduction is in agreement with the observations of Sec. 7 when relatively small current densities are passed through the insulator. At the bias levels where the intermediate impedance-level state is observed a partial inversion is observed, but only by providing a much deeper potential well to contain the minority carriers than would be necessary for an ideal MIS capacitor.

SECTION 10

THREE-TERMINAL DEVICES (EMITTER AND DOUBLE COLLECTOR)

A. STRUCTURE OF DOUBLE COLLECTOR DEVICES

Another type of three-terminal CID's has been fabricated. Its structure is shown in cross section in Fig. 44 and it is seen to have no base connection, but rather two (or more) collector terminals. Several variations of this structure have been fabricated, including devices which have the two specific insulator layers used in the "emitter-base-collector" devices: the 30 silicon-rich silicon nitride. Separation between the collector contacts has been in the range of 8-25 μm.

B. COINCIDENCE EXPERIMENTS

The initial purpose of this investigation was to observe the effect of applying pulses simultaneously to each of the collector contacts. It was expected that it would be possible to observe transitions from high- to low-impedance states of the collectors if the pulses were received in coincidence, even if no transitions were possible if they were received at different times. Experiments of this general type were performed by Chino, Suzuki and Mizushima[16] on devices which may well be more similar to the CID structure than these authors realized.

The experimental arrangement is illustrated in Fig. 45. Pulsed voltages of magnitude V_1 and V_2 are applied to the series combination of a load resistance R_L and the collector terminals themselves. If a current I_1 flows in the first collector, then $V_{C1} = V_1 - I_1 R_L$, thus, V_{C1} can be substantially lower than V_1 if the first collector has made a transition to the low impedance state.

The simultaneous triggering of two collectors to the low-impedance state was observed for pulses which could not cause transitions if they were applied individually. This behavior is illustrated in Fig. 45(a) and (b). Noncoincidental arrival of the pulses is shown in Fig. 45(a). The magnitudes of V_{C1} and V_{C2} are almost exactly equal to V_1 and V_2, indicating very small
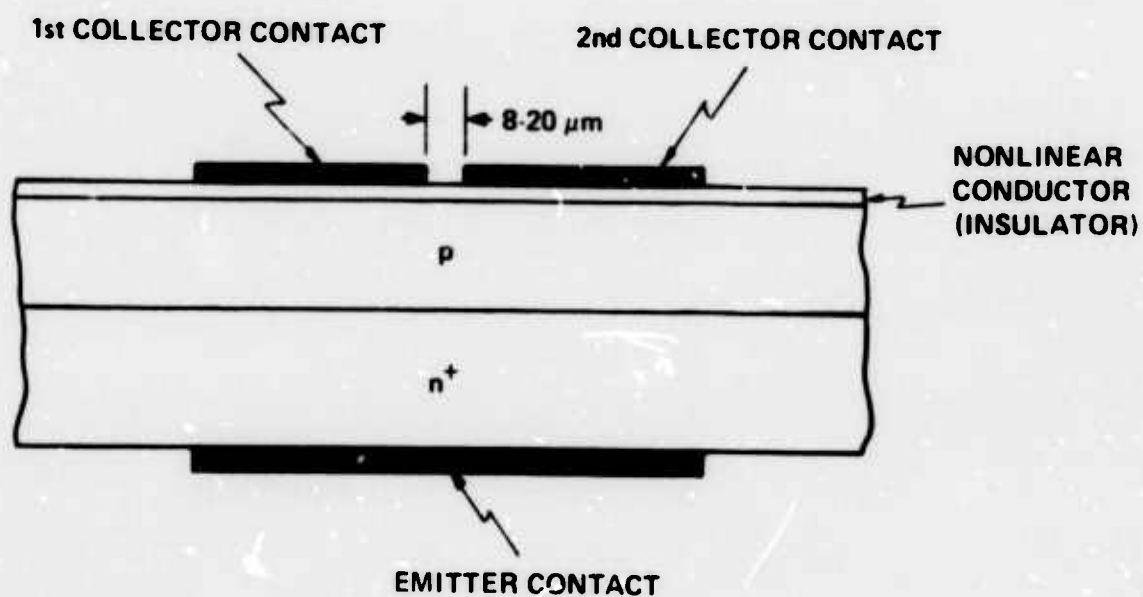
FIG. 44 Cross-sectional diagram of double-collector electrode CID structure.
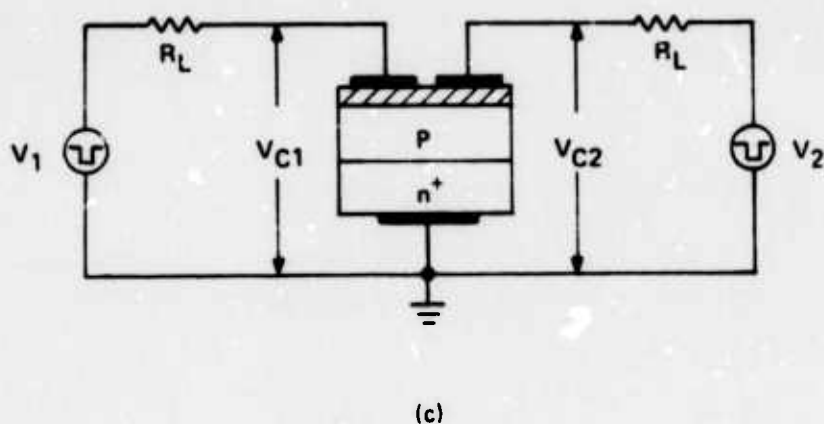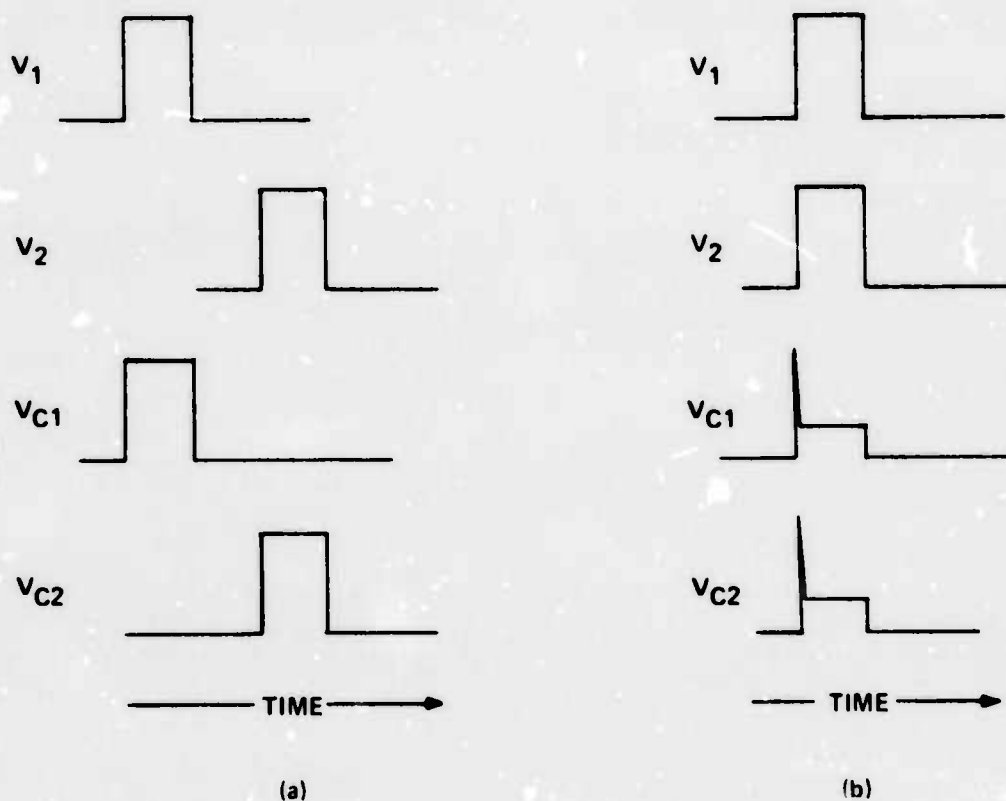
FIG. 45 Diagrams for explaining double-pulse experiments.

(a) Noncoincidental arrival of intermediate voltage level pulses. No switching to low-impedance state.

(b) Coincidental arrival of intermediate voltage level pulses. Note switching to low-impedance state for both collectors.

(c) Experimental arrangement. V_1 and V_2 are voltages applied to series combination of collector and load resistor. V_{C1} and V_{C2} are voltages at collector terminals.

current flow. The same magnitudes of V_1 and V_2 are sufficient to cause transitions of both collectors to the low-impedance state if they were applied simultaneously as in Fig. 45(b).

No interaction between pulses was observed if they were applied to collectors of two different semiconductor chips. Thus, the interaction must take place within the device itself, as distinguished from being an anomaly of our experimental arrangement. The mechanism responsible for this interaction is presumably the greater concentration of minority carriers (in this case, electrons) near the semiconductor-insulator interface caused by the application of bias to two adjacent collectors. Greater minority carrier density is known to be an aid to causing inversion and hence transition to the low-impedance state, as evidenced by the effects of base current, described earlier, and the effects of illumination.

In order to determine the criticality of the magnitude of voltage pulses which can perform this function, experiments were carried out with metal silicon nitride p-n$^+$ structures. These devices had a 23 V threshold voltage for switching to the low-impedance state if a pulse was applied only to a single collector terminal.

The experiment consisted of measuring the voltage applied to the second collector which was required to cause the first collector to switch as a function of the voltage applied to the first collector. These data are plotted in Fig. 46. From this graph it can be seen that if the voltage applied to the first collector is more than about 9 V below its threshold, then almost the full threshold voltage must be applied to the second collector in order to cause a transition. On the other hand, if less than one volt is applied to the first collector, then the voltage which must be applied to the second collector is within four volts of its threshold. Between these extremes a reasonable window exists for reliable AND function behavior, with voltages having to be controlled to within only $\pm$ 20%.

C. NONCOINCIDENTAL APPLICATION OF PULSES TO DOUBLE COLLECTOR DEVICES

In contrast to the expected results of the previous section,

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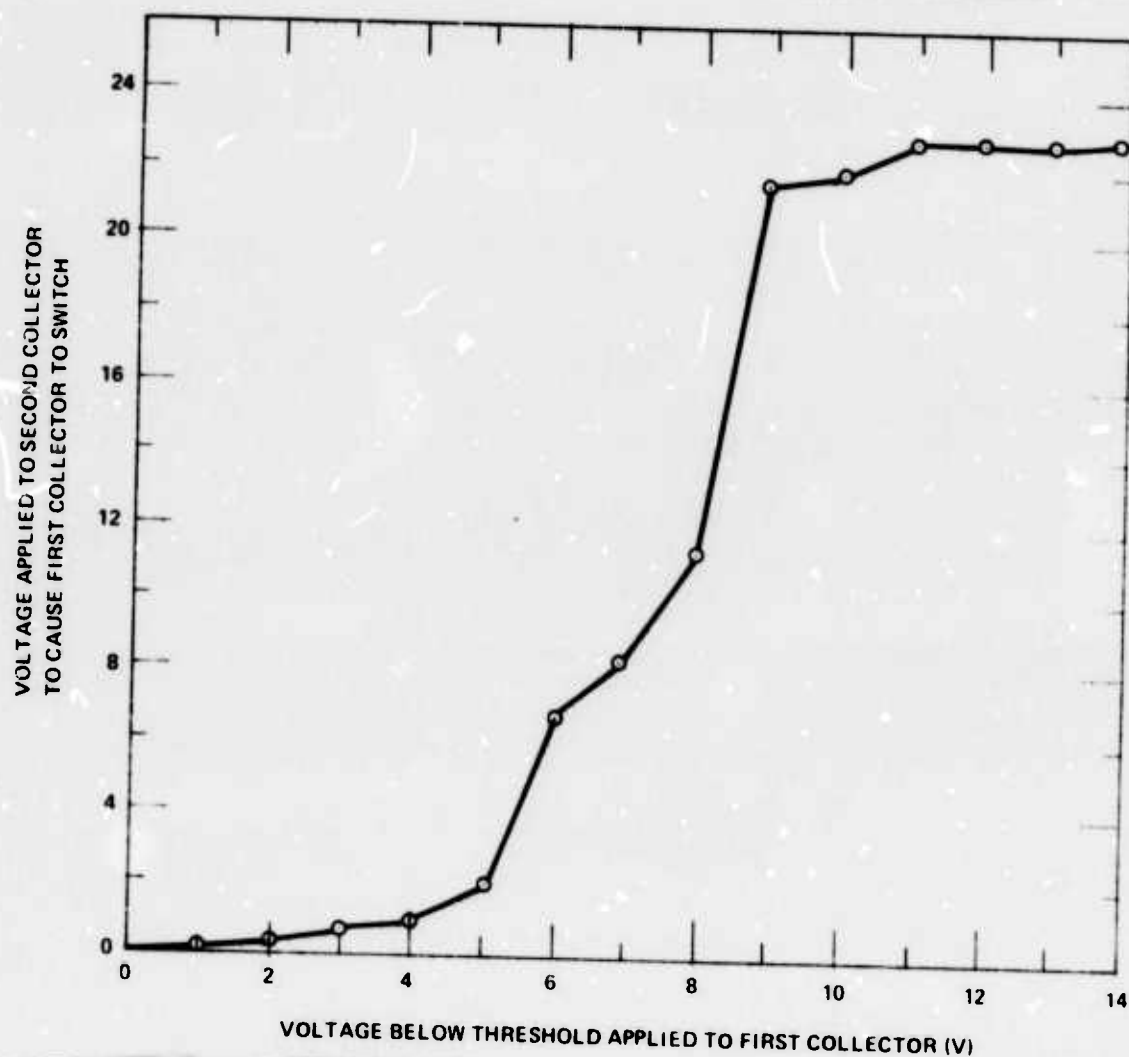
FIG. 46 Voltage required to cause switching of second collector of a double-collector CID structure as a function of voltage applied to the first collector. Separation of collectors is 8 μm.

interaction between pulses applied nonsimultaneously to both collectors of the double-base structure was also observed if the magnitude of the pulses was in the correct range. In fact, it eventually became clear that a single collector could "remember" for times of the order of a millisecond that a pulse had previously been applied to it. This result is in sharp contrast to the experiments described in Chino et al.[16]

The interaction between pulses applied at different times to a double- (or single-) collector CID is generally that of an inhibit function. The first pulse applied tends to prevent a transition to the low-impedance state of the second collector. The strength of this interaction is greater if the magnitude of the first (control) pulse is increased.

The experimental results are graphically illustrated in Fig. 47(a) and (b). Note that equal magnitude pulses are used in these illustrations; only the time sequence of the order in which they are applied is changed. In particular, note that as in (a) it is possible to find a voltage V_1 applied to one collector which will cause a transition to the low-impedance state if it is applied first (or without application of any pulse to the second collector). However, if, as in Fig. 47(a), the application of V_1 is preceded by application of a pulse to the second electrode, then no transition to the low-impedance state of the first collector takes place.

In general, the greater the magnitude of V_2, so long as it is less than V_{th}, the greater the time interval τ, defined in Fig. 47(a), over which the collector of the device can "remember" that a pulse has been applied to an adjacent electrode. We emphasize that during this time interval τ no power at all has been applied to any part of the device. In fact, very little power has to be applied to the control collector at all, since it can perform a "write" function if no transition to the low-impedance state occurs. Therefore, very little current flows during application of the pulse.

Depending upon the details of the device structure, quite different behavior can occur if the first pulse which is applied is of sufficient magnitude to cause a transition to the low-impedance state. For devices which have been fabricated using the 300 Å silicon-rich silicon nitride, for
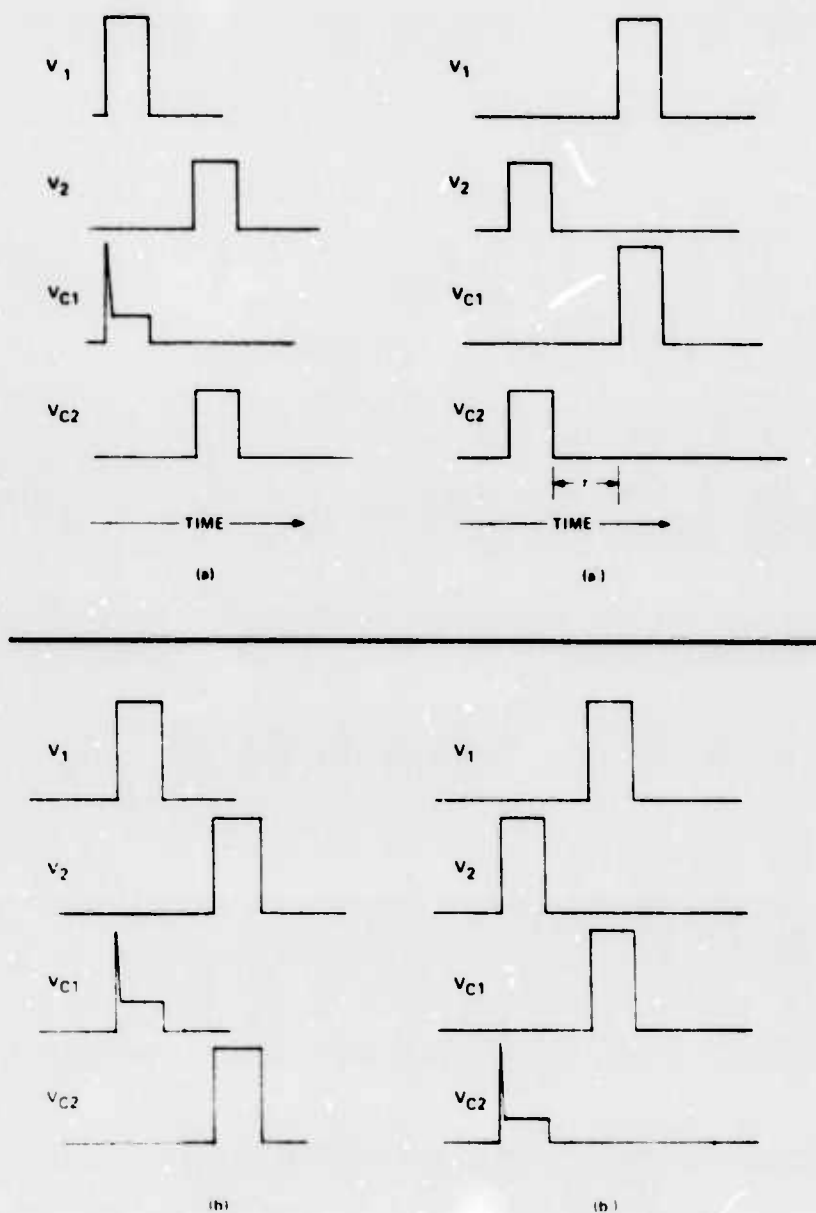
FIG. 47 Pulse sequence which illustrates inhibit function for noncoincidentally arriving pulses.

(a)   Voltage V_1 applied to first collector is sufficient to cause transition to low-impedance state. V_1 applied before V_2 applied to second collector.

(a') Voltage V_2 applied to second collector before V_1 applied to first collector. Magnitude V_1 no longer sufficient to cause transition of first collector to low-impedance state.

(b) and (b') Voltages sufficient to cause transitions to low-impedance states applied to both collectors. Only the pulse which arrives first causes a transition. Not all CID structures show this effect.

example, it is found that if the first pulse does cause a transition to the low-impedance state then no inhibiting tendency is observed when the second collector is pulsed.

On the other hand, devices fabricated using the 30 Å oxynitride show a particularly strong inhibit function if the first pulse is of sufficient magnitude to cause transitions to one of the low-impedance states. As illustrated in Fig. 47(b) and 47(b'), for this device the pulse which is applied first will cause a transition and the second pulse will not, even if the magnitudes of the pulses are equal.

The experimental results outlined above show that the device has a volatile memory of previous applications of voltage pulses (or dc bias). This phenomenon undoubtedly contributed to the difficulties we experienced in interpreting the conditions under which circuitry and biasing would affect latching/no latching and speed of switching of the three-terminal emitter-base-collector devices described previously.

It is important to note that the inhibit function caused by prior application of a pulse can be overridden. Thus, for example, if a higher voltage is applied in the second pulse, then the only effect of the first pulse is that the transition to the low-impedance state during the second pulse is slowed down. The voltage range for which this statement is true is quite limited (~ 1 V). For still higher voltages applied to the second pulse, no observable effect occurs because an earlier pulse has been applied.

D. EXPERIMENTS WITH MULTIPLE-COLLECTOR DEVICES

The mechanism responsible for the inhibit function should be understood, even though the phenomenon is not directly exploited in order that it can be completely suppressed if so desired. As noted above, there is no evidence of the inhibit function being present if two different CID chips are mounted on the same header or if the collectors on the same chip are separated by etching a groove in the semiconductor chip between the collectors. It is also reduced to almost undetectibility if the insulator is removed between electrodes. We therefore conclude that the inhibit function is not

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produced by "crosstalk" between circuit connections but involves information transfer within the device itself.

A more detailed observation of the inhibit effect is therefore necessary. In these experiments we are interested in the minimum time interval between the controlling pulse and the controlled pulse for which an inhibit function is operative. This minimum time θ is illustrated in Fig. 48. For time intervals longer than θ (but shorter than τ discussed in the preceding section and illustrated in Fig. 47), the controlling collector can inhibit the transition of the controlled collector to the low-impedance state. If any shorter time interval is used, as in the bottom illustration of Fig. 48, then the second collector will undergo a transition to the low-impedance state for at least part of its pulse. The definition of θ is, of course, somewhat arbitrary. One could define θ as that time interval for which the controlled collector makes as rapid a transition to the low-impedance state as it would if the controlling pulse were not applied, rather than making any transition at all during its duration. The latter definition was chosen because it could be measured with greater objectivity. In order to limit uncertainties, short pulses were used. Pulse lengths of 100 ns and 300 ns were used for the controlling and controlled pulses, respectively.

The original device structure in which the inhibit function was observed had a narrow collector separation, as illustrated in Fig. 44. For the narrow collector separation of 8-20 μm for this device, θ was essentially zero. A new structure was therefore required and a different mask (illustrated in Fig. 49 was used to produce an array of fifty different collector contacts on a single chip. By choosing to contact any particular pair of electrodes, the spacing could be varied from 10-1300 μm. A typical arrangement is shown in the photograph of Fig. 50. With collector separations of 650 μm, the inhibit pulse had to be applied and removed about 0.25 μs before the initiation of the second pulse, for a 1300 μm collector separation, the inhibit pulse had to be applied and removed about 1.5 μs before the start of the second pulse. This qualitative determination of θ shows that the mechanism is too fast for simple diffusion over such large distances. One would expect
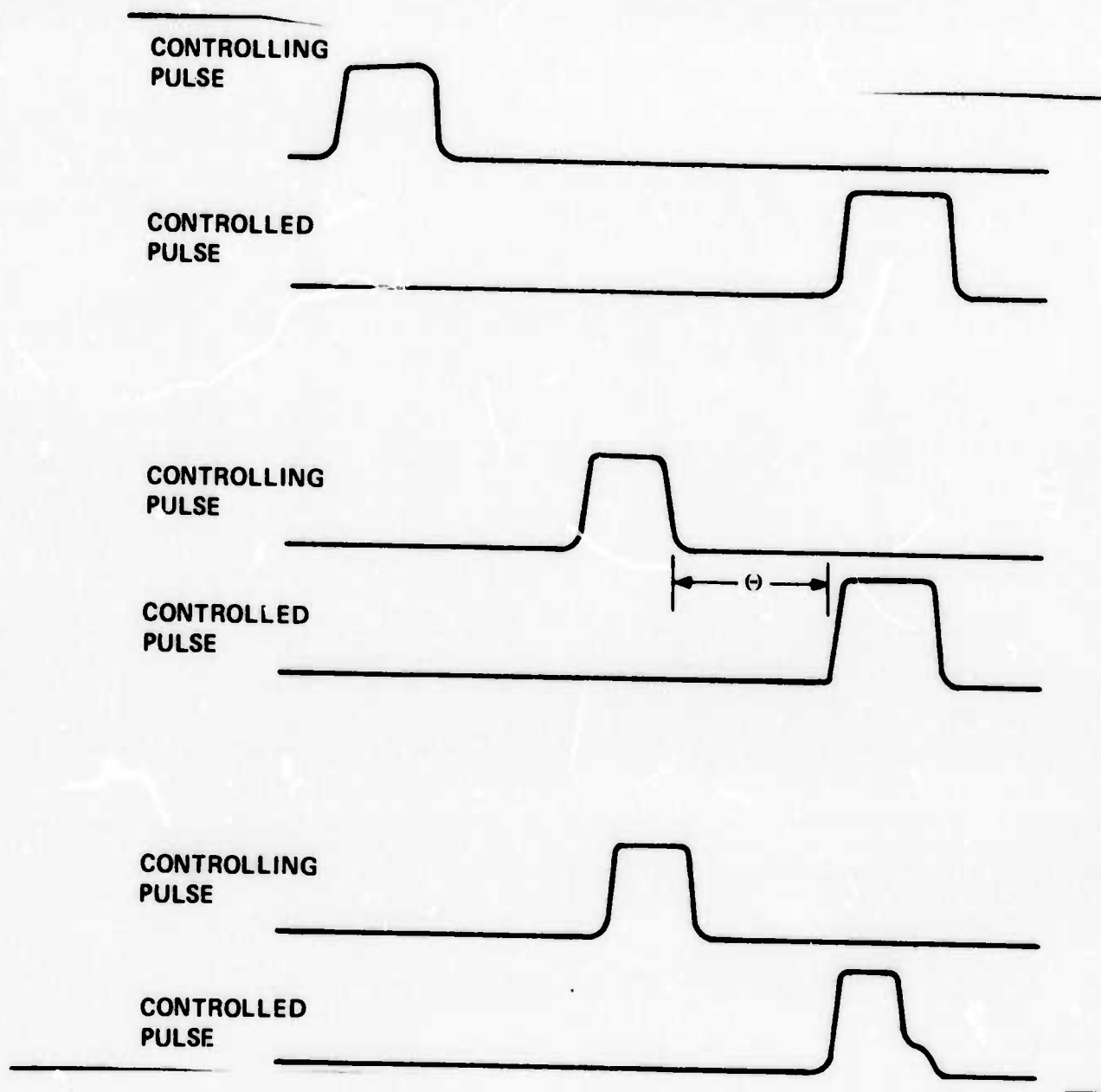
FIG. 48 Graphical definition of Θ, the minimum time interval between controlling and controlled pulses which is necessary for controlling pulse to completely inhibit transition of controlled pulse to low-impedance state. In top illustration inhibition is complete. For the time interval Θ is shown in middle illustration; inhibition is also complete, but for any shorter time interval, as shown in bottom illustration, a transition to low-impedance state of controlled collector will occur.
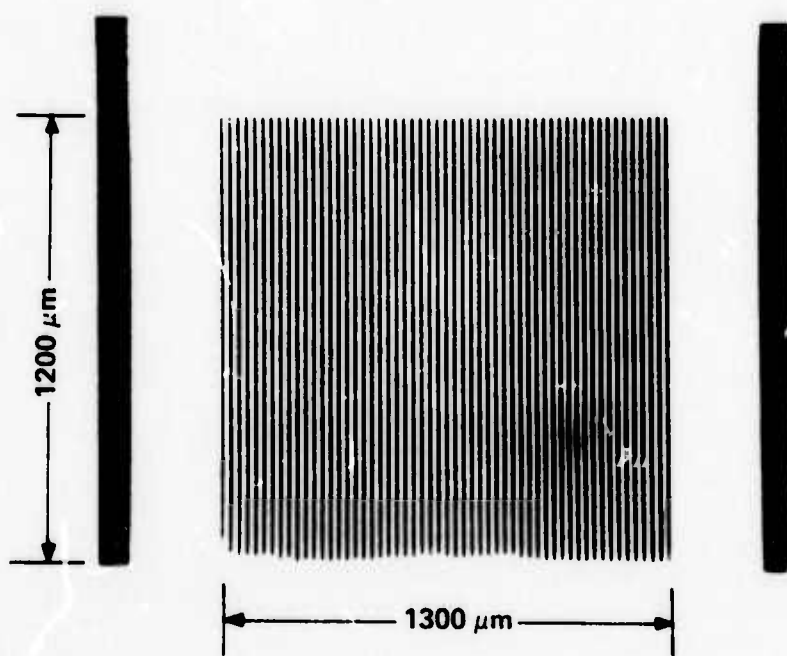
FIG. 49 Photomicrograph of the mask used to produce the multicollector CID structure with large separations between collector electrodes.

FIG. 50 Photomicrograph of multiple-collector CID structure. For this device three collectors were contacted, including two near the widest possible separation and one near the middle.

that for a distance of 1300 μm, simple diffusion would yield a time of the order of $\ell_2/D = (1.3 \times 10^{-1})^2/40 \sim 4 \times 10^{-4}$, which is two order of magnitude greater than what was observed. In the above estimate, we have taken the diffusion coefficient of electrons to be 40 cm^2/c.

In practice, it is found that a measurement of θ will depend upon the magnitudes of the voltage pulses which are used in the experiment. We present data on how a θ varies with changes in the controlling collector's pulse voltage when the magnitude of the controlled collector voltage pulse is kept constant. These data are plotted as the reciprocal of θ as a function of the controlling collector voltage for collector separation of 1160 μm (Fig. 51) and 284 μm (Fig. 52). As illustrated in these figures, it is always observed that a higher voltage must be applied to a controlling collector to enable it to inhibit a transition of a controlled collector if the separation between collectors is greater. This indicates that the strength of the interaction falls off with separation. Larger values of θ can always be achieved with greater collector separation. The data which represent the largest values of $1/\theta$ are less meaningful because the arbitrary aspects of the definition of θ are more significant. Data cannot be continued to lower values of $1/\theta$ than that which is presented because the inhibit function becomes too weak to detect at smaller controlling collector voltage.

These data do not support any simple diffusion explanation of the inhibit function. The absence of the inhibit function for polysilicon insulating layers, mentioned above, also does not fit with a simple diffusion explanation. The explanation of the inhibit function remains uncertain beyond an assertion that it involves something within the device structure itself. That "something" could simply be the propagation of a signal at the speed of light within the semiconductor, with the apparent delay being caused by a damping of the signal over longer paths of propagation with the consequence that one must wait longer for the signal to build up at the controlled electrode if it is further away from the transmitting electrode. This specu-lation supposes that the signal has an amplitude which increases with time over an interval which is at least as large as the measured value of θ.
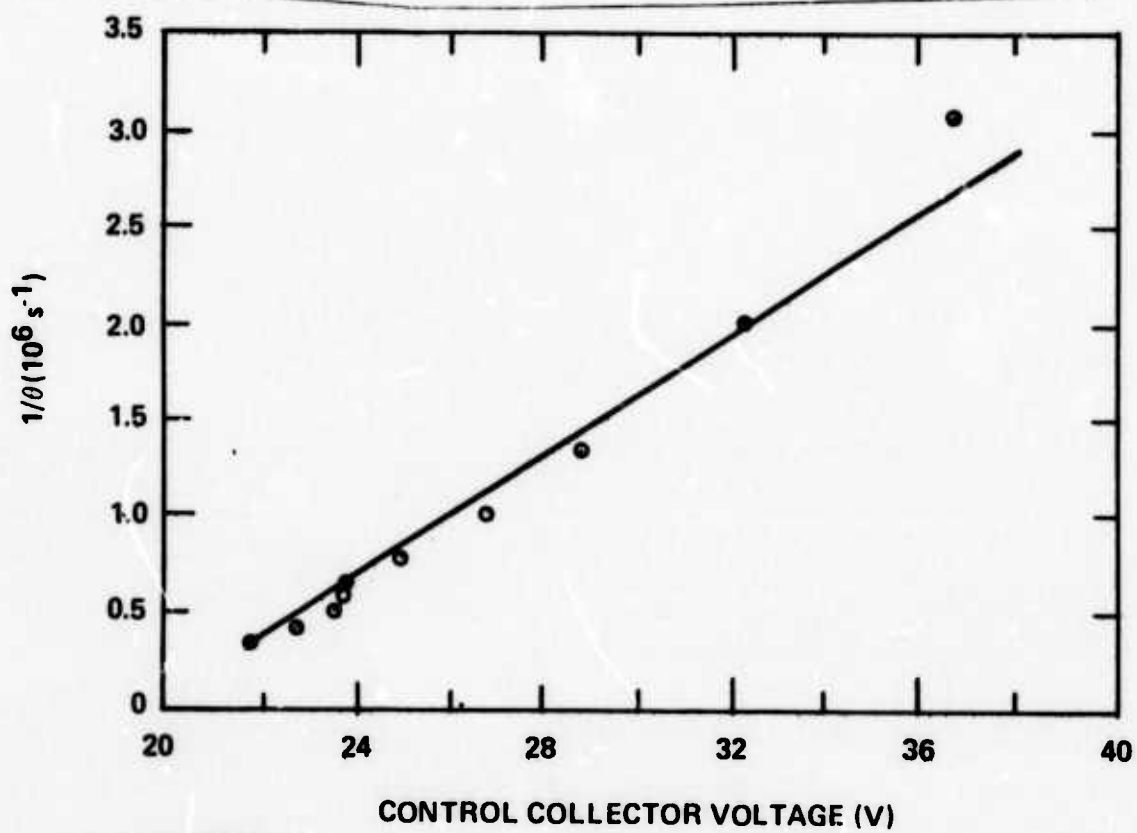
FIG. 51 Reciprocal of minimum time interval between controlling pulse and controlled pulse as a function of controlling collector's pulse voltage for collector separation of 1160 μm. Controlling and controlled pulse widths are 100 and 300 ns, respectively.
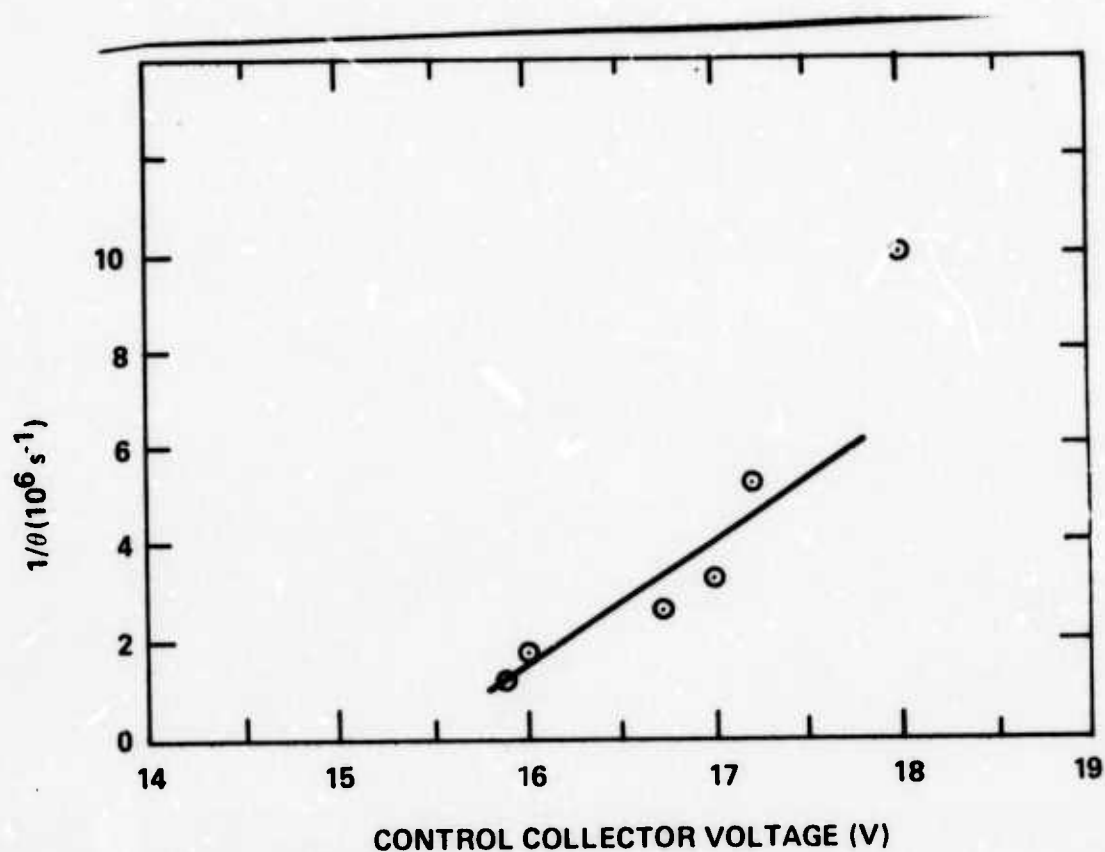
FIG. 52 Reciprocal of minimum time interval between controlling pulse and controlled pulse as a function of controlling collector's pulse voltage for collector separation of 284 μm. Controlling and controlled pulse widths are 100 and 300 ns, respectively.

This speculation receives some support from experiments which monitor the voltage at the "controlled" electrode instead of applying a pulse which may trigger a transition. Figure 53 presents measurements of the transient voltage detected at a second electrode as a result of a pulse applied to the "first" electrode. Note that the receiving electrode's signal builds up for at least 20 µs after the transmitting electrode has fired. The received signal is also greatly reduced if the chip il illuminated. Illumination also cuts down on the strength of the inhibit effect. Greater separation between electrodes does not qualitatively change the shape of the received signal.

In conclusion, it has been demonstrated that the inhibit function operates over distances on the semiconductor chip in which one would hope to pack many devices. Isolation either by diffusion or the use of polysilicon or amorphous insulator layers, rather than nitrides, or complete removal of uncovered insulation would therefore appear to be mandatory for integrated circuit applications.

1st ELECTRODE
VOLTAGE

2nd ELECTRODE
VOLTAGE

(a)

TIME (10 μs/div) ⟶

1st ELECTRODE
VOLTAGE

2nd ELECTRODE
VOLTAGE

(b)

TIME (10 μs/div) ⟶

FIG. 53 Oscilloscope traces of voltage pulse applied to a "transmitting" electrode and observed voltage at a second "receiving" electrode of a multiple-collector CID structure. The voltage scale for the transmitting electrode is 10 V/div while the voltage scale for the receiving electrode is 50 mV/div. (a) Device is dark. (b) Device illuminated with strong tungsten source.

SECTION 11

OBSERVATIONS OF NONVOLATILE MEMORY PHENOMENON

A. DESCRIPTION OF BASIC STRUCTURE AND METHOD OF FABRICATION
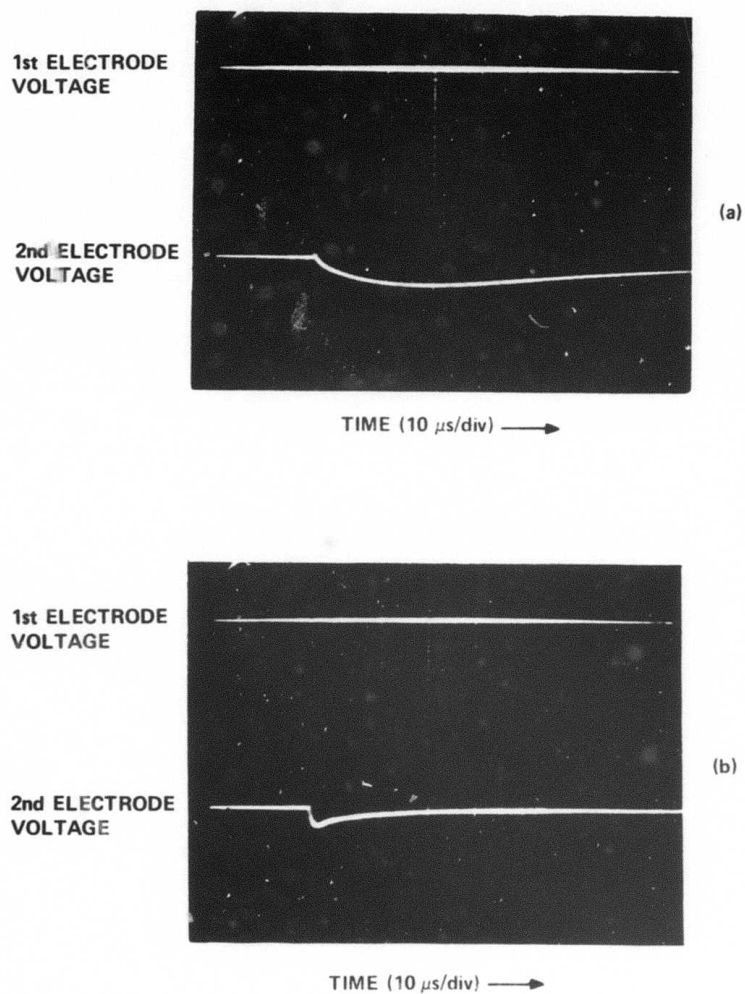
The basic CID phenomenon required a p-n junction, a nonlinear conductor (insulator) and a high-conductivity collector. As described in Sec. 3, polysilicon can be used as both the insulator and the primary collector contact. Since it is possible to fabricate p-n junctions of polysilicon, the question naturally arises as to whether the entire CID structure can be fabricated from polysilicon. The structure of Fig. 59(a) was therefore produced in order to test this hypothesis.

The structure of Fig. 54(a) clearly requires no single crystal silicon. It is produced by first sputtering 2000 Å of molybdenum on a polished fused quartz substrate. The freshly deposited molybdenum was quickly transferred to the silicon reactor and, following flushing with argon, the substrate was heated in pure hydorgen at 850°C for 20 minutes. The temperature of the reactor was then reduced to 700°C and the layers were deposited sequentially without removing the quartz substrate from the reaction chamber. The n^+ layer was deposited with phosphorus-doped silane with hydrogen and argon as the carrier gas. The p layer was deposited similarly, but with diborane-doped silane. The insulating polysilicon layer was deposited with undoped silane using only argon as the carrier gas; the final p^+ layer was deposited similar to the p layer, but using silane more heavily doped with diborane.

The structural variations of Fig. 54(b) and (c) were fabricated by similar means, with each structure begun by heating in hydrogen and each corresponding layer deposited by exactly the same methods used for the structure of Fig. 54(a). These variations in structure were produced to help elucidate the phenomena observed in the basic complete polysilicon CID structure of Fig. 54(a).
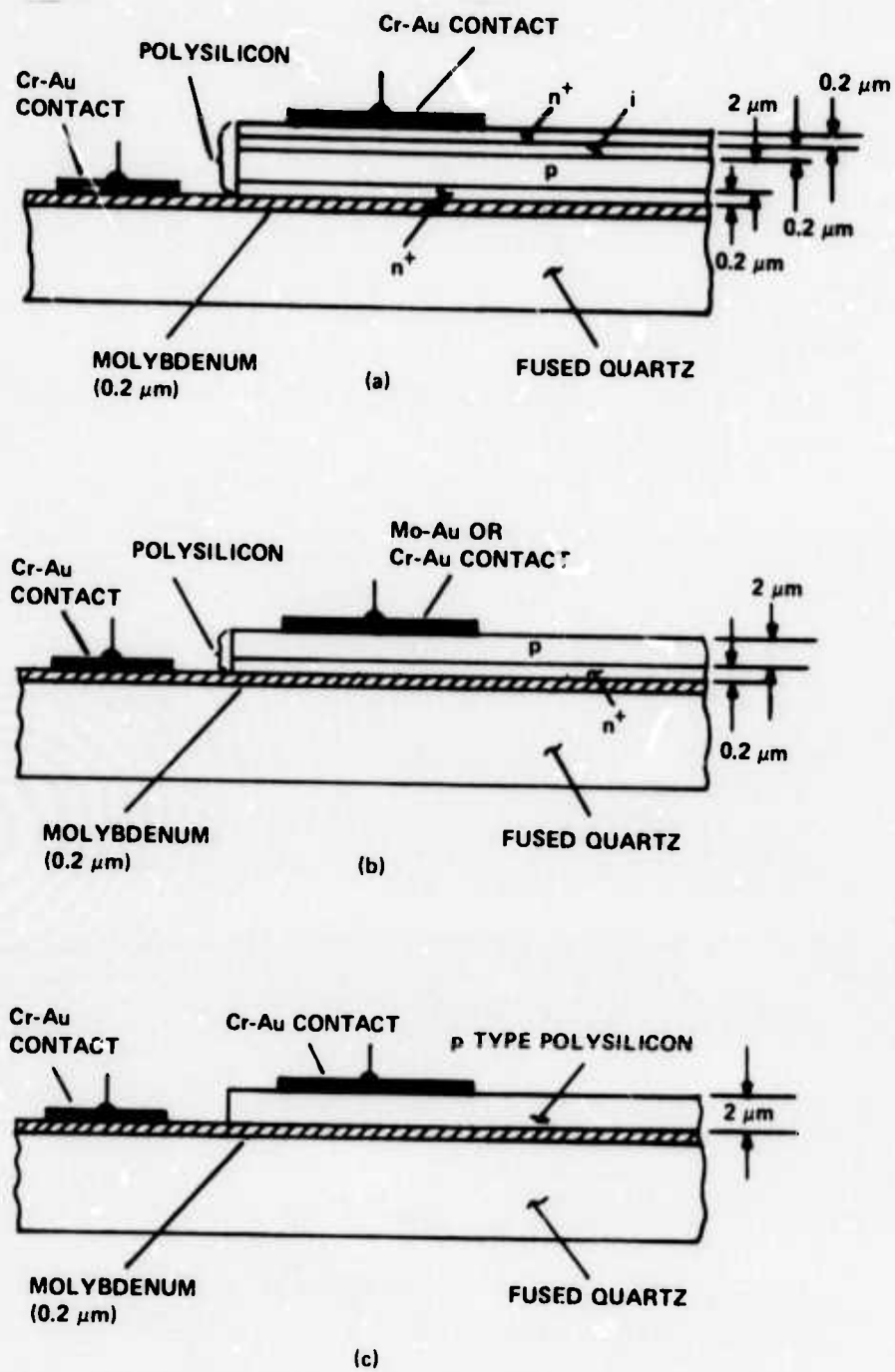
FIG. 54 Cross-sectional diagrams of three device structures fabricated using no single crystal silicon:

(a) Complete polysilicon analog of CID;

(b) Structure for polysilicon p-n junction evaluation;

(c) Single-layer p-type polysilicon device.

B. BASIC PROPERTIES OF COMPLETE POLYSILICON STRUCTURES

The I-V characteristics of the structure of Fig. 59(a) were investigated. The devices showed the existence of a virgin state whose I-V characteristics are shown in Fig. 55(a). If a large enough voltage is applied to the device in the virgin state, a change occurs in the I-V characteristics of Fig. 55(b). Note that a negative resistance is present, with a turn-over voltage significantly lower than that which may be applied to the virgin state. This change from the virgin state is brought about by a sense of voltage which forward biases the p-n junction, the same sense of voltage which is applied to a conventional CID structure.

This nonvirgin state of the device may be reversibly altered by applying a voltage in the opposite sense. The I-V characteristic appears as in Fig. 55(c) after a sufficiently great "reverse" bias is applied to the device. This "written" state is one which shows linear conductivity at low voltages. The "written" state may be "erased" by again applying a voltage which forward biases the p-n junction. Alternation between this "written" and "erased" state may be continued apparently indefinitely.

C. EXPERIMENTS ON STRUCTURAL VARIATIONS OF THE BASIC DEVICE

The two variations of the basic CID structures shown in Fig. 54(b) and (c) were fabricated in order to help explain the mechanisms of the device behavior described above. The simple p-n junction structure of Fig. 54(b) was actually fabricated before the behavior of the basic CID-type structure of Fig. 54(a) was observed in order to evaluate the polysilicon p-n junctions. The simpler p-n junction structure of Fig. 54(b) also showed a virgin state and an ohmic "written" state, as well as an "erased" state with higher impedance (with negative resistance) at higher voltage.

As with the complete $n^+/p/i/p^+$ structure, the virgin state was removed by applying a voltage which forward biases the p-n junction. The virgin state could not consistently be removed without permanently damaging the device if a voltage was applied which reverse biased the p-n junction. As with the complete four-layer structure of Fig. 54(a), the ohmic low-
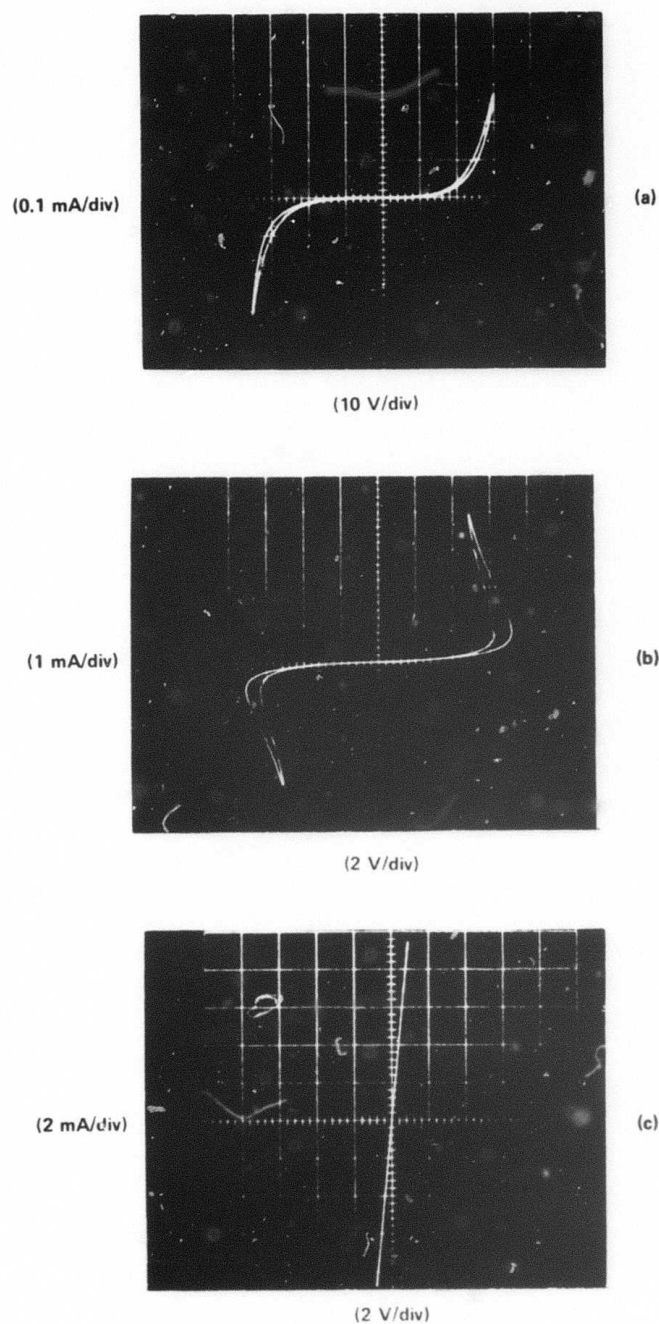
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FIG. 55 I-V characteristics of metal/p^+/i/p/n^+/moly devices. All semiconductor layers were formed with polysilicon. (a) Virgin state. (b) "Erased" state. (c) "Written" state.

resistance state was produced by applying a voltage to the nonvirgin sample which reverse biased the p-n junction. The virgin, "erased" and written states of the moly/n^+/p/metal device are illustrated in Fig. 56(a), (b) and (c).

The nonvirgin states of the devices tend to be fairly symmetric about the origin of the I-V curves. Figure 57 is a composite sketch of both the "erased" and "written" states of the device, with arrows showing the critical transition points from one curve to the other. The simple moly/n^+/p/metal structures had I-V characteristics which were more like each other than did the original moly/n^+/p/i/p^+/metal structures. In addition, the simpler structures were less fragile, presumably because lower output power was required to remove the original virgin state and to accomplish the "writing" and "erasing" processes. For these reasons, the simpler moly/n^+/p/metal structures were chosen as the standard structure for further investigation of this nonvolatile memory behavior.

An even simpler structure was studied briefly. This was the moly/p/metal structure of Fig. 54(c). This device structure showed qualitatively the same states as the other two structures, but had a much lower resistance in its "off" ("erased") state. The I-V characteristics of the device in its virgin state are shown in Fig. 58(a) and both its "erased" and "written" states are shown in Fig. 58(b). Because there was a much smaller resistance difference between the "written" and "erased" states of this device it was viewed as not having as good a device potential and has not been investigated further.

D. FURTHER OBSERVATIONS ON BEHAVIOR OF MOLY/n^+/p/METAL DEVICES

Several runs of moly/n^+/p/metal devices have been fabricated since this structure was chosen for further investigation. The properties of these devices have proven repeatable from run to run. Typical resistances of devices in the "written" state are 40-50 Ω and typical resistances in the "erased" state are 50-250 $K\Omega$ for devices having areas of 1.25×10^{-4} cm^2. The n^+ layers were typically 2000 $\overset{\circ}{A}$ thick and the p layers were approximately

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FIG. 56 I-V characteristics of metal/p/n$^+$/moly device. Both **semiconductor** **layers** were formed with polysilicon. (a) Virgin state. (b) Erased **state.** (c) Written state.

FIG. 57 Detailed sketch of I-V characteristics of metal/p/n⁺/moly device. Load
lines show transitions between the two different impedance states.
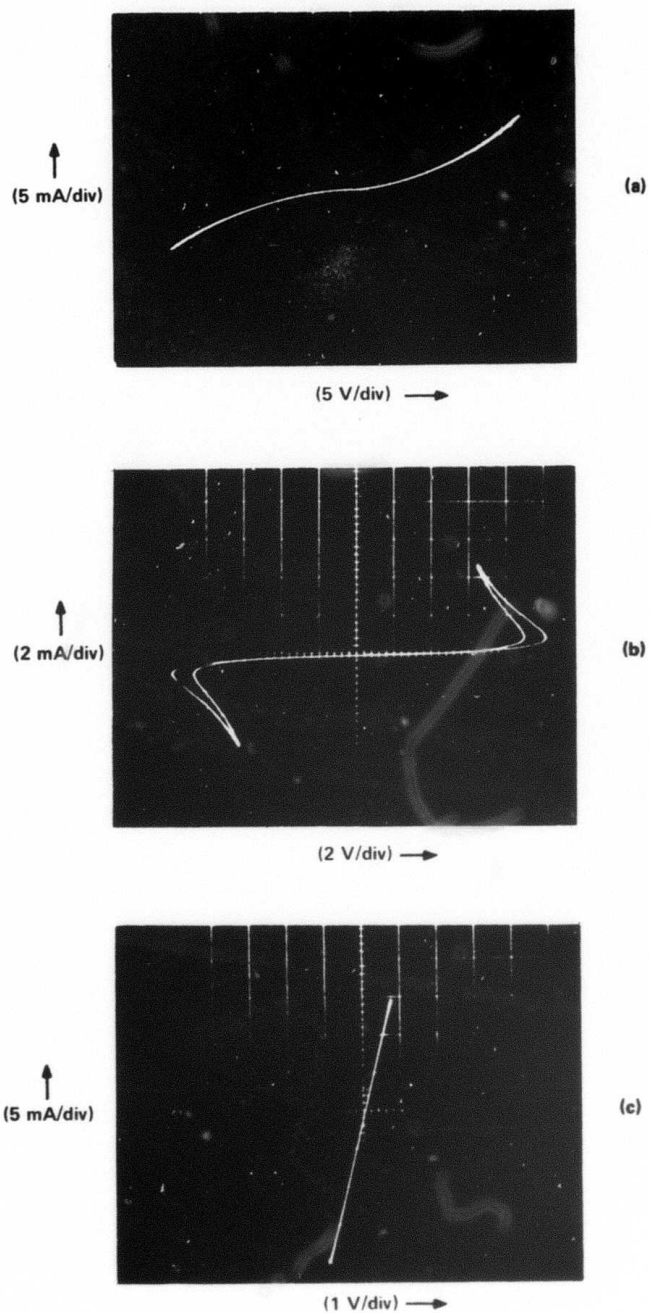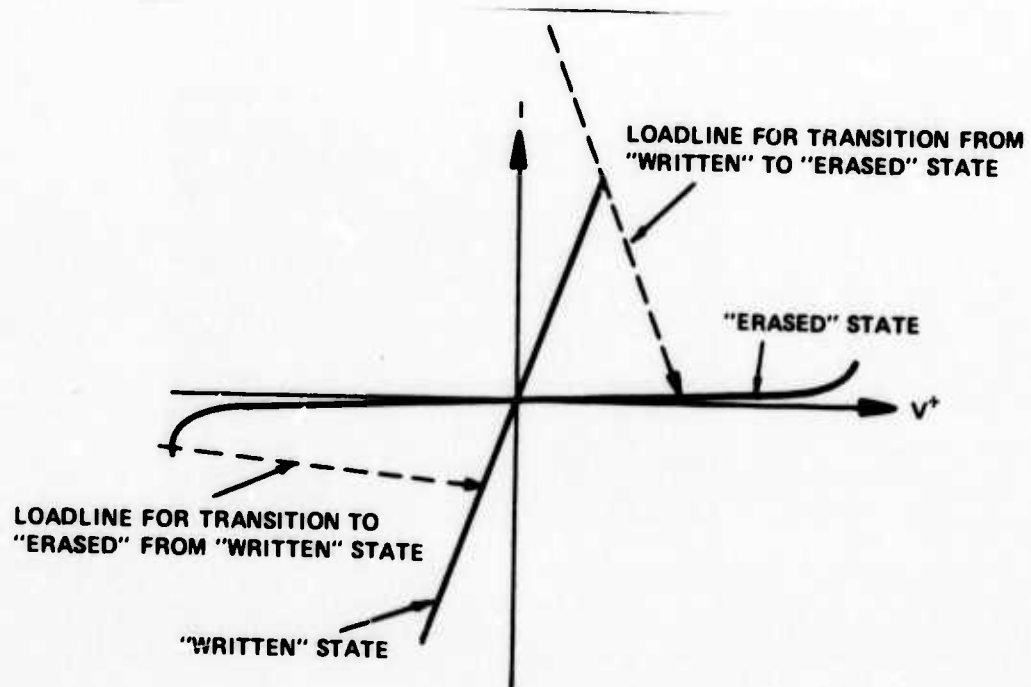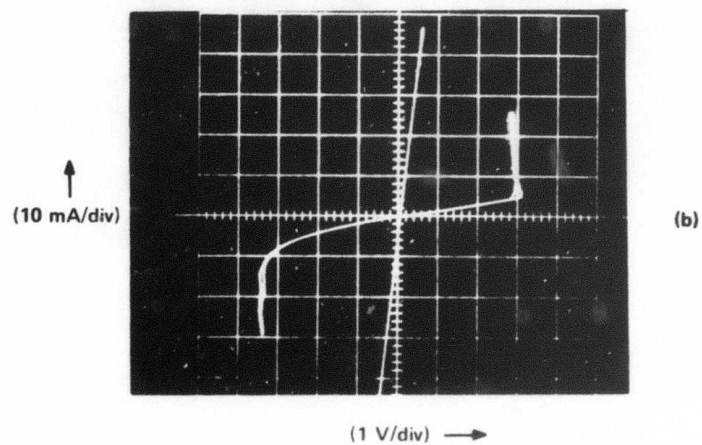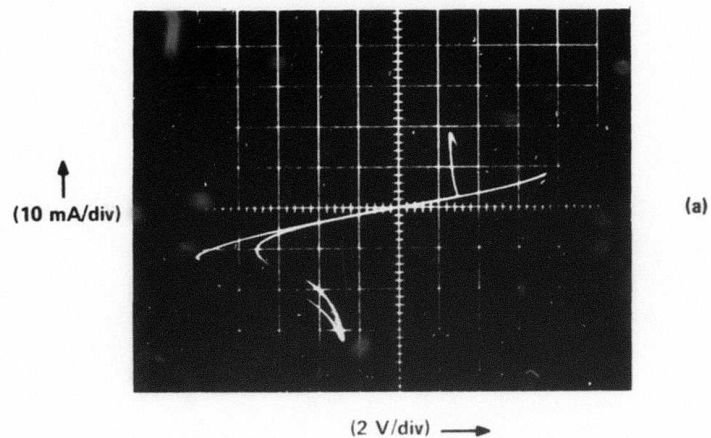
(10 mA/div)

(a)

(2 V/div) →

(10 mA/div)

(b)

(1 V/div) →

FIG. 58 I-V characteristics of metal/p/moly device. The semiconductor layer is polysilicon. (a) Virgin state. (b) Erased and written states.

2 μm thick. Three different metallization procedures were chosen for the top electrode: evaporated chromium-gold, sputtered molybdenum-gold and sputtered molybdenum-gold which had been preceded by a sputter etching of the p-type polysilicon layer. All three metallization procedures resulted in the same device behavior.

The "erased" and "written" states were more or less binary. Some further lowering of the impedance of the "written" state is possible if it is written harder; some further raising of the impedance of the "erased" state is possible if it is erased harder, but it is not possible to obtain an intermediate level of impedance at low applied voltages. Devices have retained their "erased" and "written" characteristics for days without any observable change in low-voltage impedance when stored at room temperature with no applied bias.

Raising the device's temperature to 90-120°C caused a partial erasure of the low-level impedance state. Prolonged storage (1-2 hours) at 250°C resulted in complete erasure of the written state. No change in state was observed if the devices were cooled to 77°K. The turn-over voltage to negative resistance in the erased state increased about 10-20%, however, when the devices were cooled. A higher imput power is therefore required to "write" the devices into their low impedance state. Devices cooled to liquid nitrogen temperature appeared to be slightly easier to erase than if the process was attempted at room temperature.

Devices have been cycled between low- and high-impedance states hundreds of times without changing either the "written" or "erased" I-V characteristics. It is important to limit the power dissipation in the writing and erasing processes if the device is to be undamaged. The load lines suggested in Fig. 57 are useful for this purpose, with a high-impedance load resistor used to bring the devices from high- to low-impedance states and a low value of load resistance used to bring the device from low- to high-impedance states.

The devices may be transferred between the two impedance states by single-shot pulsing as well as by using a conventional 120 Hz transistor

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curve tracer. At room temperature the single-shot pulsing of the device to accomplish the "writing" operation requires a pulse no longer than 50 ns (shorter pulses have not yet been attempted). The "erasing" operation requires pulses in the range from 10-25 μs, however. The reason for this discrepancy is not understood.

If either the "write" or the "erase" operation was accomplished by pulsing, then the device was more completely "erased" or "written" than it would have been using a curve tracer power supply at the same peak current and voltage. This result was somewhat surprising since clearly less total power is dissipated in the device in single-shot pulsing than in multiple cycles of the curve tracer. The current and voltage levels of both the pulsed power supply and the sawtooth waveforms of the curve tracer were care-fully calibrated to be certain that the peak current or voltage of the single-shot pulse was always less than the curve-tracer peaks. The "completeness" of the erasure or writing process was measured quantitatively by determining the minimum current (or voltage) which must be supplied by the curve tracer in order to undo the previous process.

No exception to the observation that these processes are more com-olete when performed by the pulses than by the curve tracer has been dis-covered. Very preliminary results indicate that pulse shaping can remove at least some of this discrepancy. Pulse writing and erasing can be per-formed less completely if slower rise and fall times of the pulses are used by applying the output of the pulser to appropriate R-C networks so that the high-frequency components of the pulse are not applied to the device.

SECTION 12

HIGH CURRENT DENSITY DEVICES

Recently fabricated devices have been found to be able to carry $1-2 \times 10^3$ A/cm^2 in the high conductivity state. Certain of these devices have been able to carry $2-5 \times 10^3$ A/cm^2 without permanent damage but with some temporary reduction in threshold voltage due to heating. This represents about an order to magnitude improvement in maximum current density over the values observed in the first devices fabricated.[1]

The improvements were not sought purposefully, so it is difficult to be sure why they did occur. Probably some improvement resulted from improvements in the practical arts: lower power sputtering of metal contacts, minor variations in cleaning wafers before nitride deposition and variations in oxynitride deposition procedure.

SECTION 13

SUMMARY OF REPORT

A. TECHNICAL PROBLEM

The controlled inversion device (CID) is a novel semiconductor device which can perform rapid switching and memory functions. It is inherently simple, having at most one p-n junction, and its fabrication can be consistent with LSI processing. The technical problem which this program addresses is to find the theoretical and practical limitations of the CID phenomenon. Only if ultimate limits to switching speed, current handling capability in the low-impedance state and packing density in integrated circuits are known can truly meaningful recommendations be made to the DOD on preferred applications of this device.

B. GENERAL METHODOLOGY

The basic method followed in discovering limits to device performance was to fabricate devices and perform measurements on important properties (swtiching speed, threshold voltages, etc.). These data were compared to the existing qualitative theory of CID operation and used to help refine this theory so it can become a quantitative description of the device behavior. Certain measurement techniques that were used are unusual in their specific application. For example, the use of microwave network analyzer techniques to measure capacitances of devices, as described in Sec. 6, represents a departure from common practice which usually makes use of frequencies no higher than about 1 MHz. It is anticipated that this technique will, for the CID structure, eventually yield valuable information regarding its response to signals which change rapidly on a time interval of a nanosecond or less. The current-voltage measurements on three-terminal CID structures, described in Sec. 7, are eventually expected to provide the first definitive information on carrier transport mechanisms across thin film insulators in metal-insulator-semiconductor structures. The capacitance-voltage measurements described in Sec. 5 have provided the first definitive information on the formation of an incipient inversion layer.

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C. TECHNICAL RESULTS

Devices have been fabricated in which a small current (supplied to the base terminal) can cause the switching of a much larger current (100-10,000 times greater) in the device's collector circuit. The collector impedance level is reduced by a factor of 10^4-10^6 during this switching. Depending upon the circut, removal of the small base current drive can result in latching of the collector to a low-impedance state in what is essentially a memory writing function, or the rapid return of the collector to a high-impedance level in what is a switching function.

Devices fabricated with polysilicon insulator layers have yielded the most reproducible devices to date, in the sense that all devices have their threshold voltages within a narrow range. These same devices showed only high- and low-impedance (no intermediate) states as well as the largest current gain observed ($\sim 10^4$).

Devices have been fabricated which can handle greater current desnities in the low-impedance state than were observed previously. Allowable current densities of 1000-5000 A/cm^2 have been observed. Currents of 0.2 to 1.0 A have been applied to such devices without damage.

A new phenomenon has been observed in devices which have no single crystal silicon, but are fabricated only from polysilicon and metal. These devices can perform a nonvolatile memory function with no input power for a time period of at least a week. Application of a voltage pulse in the reverse sense of usual CID biasing brings the device to a low-impedance state. Application of an applied pulse in the opposite sense restores a high impedance state. The impedance levels of these states can differ by as much as a factor of 5×10^3.

The use of microwave network analyzer techniques to measure high frequency capacitance of the devices has yielded interesting data. This technique has been able to supply valuable information on the subnanosecond response of these devices.

Measurements of collector efficiency of devices biased both in the usual CID sense and with inverted biasing have produced some surprising data regarding the sign of the charge carriers which cross the thin insulator structures. These techniques have begun to yield definitive data on the type of carrier (electron or hole) which predominantly crosses the insulator-semiconductor interface during conduction processes.

D. DOD IMPLICATIONS

The implications to DOD of this research on what is still a relatively new device are of necessity still speculative at present. Nevertheless, certain implications can be formulated.

The large current gain (small currents effectively closing switches which pass currents 100-10,000 times greater) confirms the expectations that these devices can be used in logic applications. Specific use could be made of this phenomenon, for example, in crossbar switching matrices whose structure is simpler than what presently available technology permits. The current gain also would permit low power write signals for memory applications.

The information on carrier transport mechanisms across the insulator-semiconductor interface could have implications beyond the CID phenomenon. Such data could contribute to improved understanding of the MNOS (metal-nitride-oxide-semiconductor) memory phenomenon. The Army, Navy and Air Force have supported development of the MNOS concept because of its nonvolatility and radiation resistance as a possibly preferred form of semiconductor memory for future systems.

The high current density capability of the CID, which has been recently demonstrated, has shaken our early hunch that the CID would not find application in power circuits. It is not yet clear that power applications are desirable, but such applications now seem possible.

The nonvolatile memory phenomenon could be of importance to DOD programs. Further work must be accomplished to establish the mechanism responsible.

E.   IMPLICATION OF FURTHER RESEARCH

The experiments on discovering the mechanism of the nonvolatile memory effect, described in Sec. 11, will have impact on future recommendations which we will make. It is possible, for example, that this phenomenon can be exploited in a fast, simply constructed, nonvolatile memory. Lacking a complete understanding of the mechanism, we are at present unable to draw definite conclusions regarding its device potential.

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